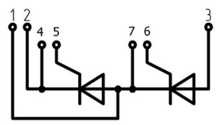
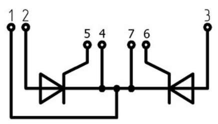
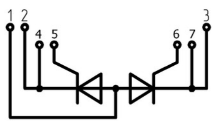
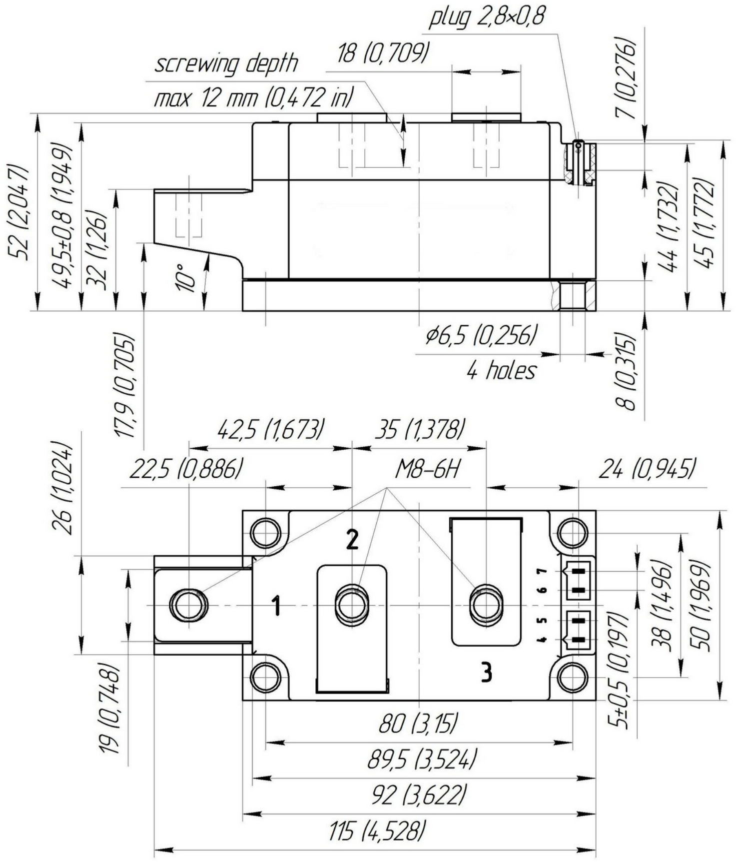
Double Thyristor Module For Phase Control
MTx-160-36-C1

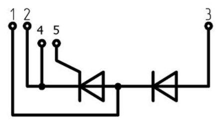
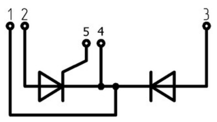
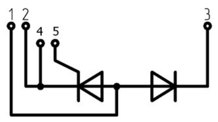
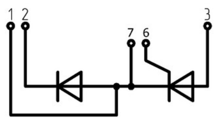
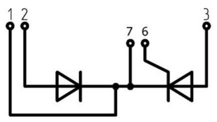
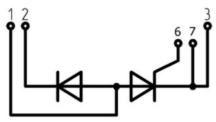
Electrically isolated base plate
Industrial standard package
Simplified mechanical design, rapid assembly
Pressure contact

Mean on-state current	I_{TAV}	160 A
Repetitive peak off-state voltage	V_{DRM}	3000...3600 V
Repetitive peak reverse voltage	V_{RRM}	
Turn-off time	t_q	400 μs

V_{DRM}, V_{RRM}, V	3000	3200	3400	3600
Voltage code	30	32	34	36
T_j, °C	–40...+125			

MT3		**MT4**		**MT5**	
					



					
MT/D3	**MT/D4**	**MT/D5**	**MD/T3**	**MD/T4**	**MD/T5**

All dimensions in millimeters (inches)

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current	A	160 169	T_c=88 °C; T_c=85 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	251	T_c=88 °C; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	4.0 4.5	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; $V_D=V_R$=0 V; Gate pulse:$I_G=I_{FGM}$; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			4.0 4.5	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; $V_D=V_R$=0 V; Gate pulse:$I_G=I_{FGM}$; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
I^2t	Safety factor	$A^2s{\cdot}10^3$	80 100	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; $V_D=V_R$=0 V; Gate pulse:$I_G=I_{FGM}$; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			60 80	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; $V_D=V_R$=0 V; Gate pulse:$I_G=I_{FGM}$; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3000...3600	$T_{j\,min} < T_j < T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3100...3700	$T_{j\,min} < T_j < T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6{\cdot}V_{DRM}$ $0.6{\cdot}V_{RRM}$	$T_j=T_{j\,max}$; Gate open	
TRIGGERING					
I_{FGM}	Peak forward gate current	A	6	$T_j=T_{j\,max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	3	$T_j=T_{j\,max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	200	$T_j=T_{j\,max}$; $V_D=0.67{\cdot}V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=I_{FGM}$; V_G=20 V; t_{GP}=50 μs; di_G/dt=2 A/μs	
THERMAL					
T_{stg}	Storage temperature	°C	–40...+50		
T_j	Operating junction temperature	°C	–40...+125		
$T_{c\,op}$	Operating temperature	°C	–40...+125		
MECHANICAL					
a	Acceleration under vibration	m/s^2	50		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.50	T_j=25 °C; I_{TM}= 785 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.20	$T_j=T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	2.300		
I_L	Latching current, max	mA	700	T_j=25 °C; V_D=12 V; Gate pulse: $I_G=I_{FGM}$; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	50 2.50	$T_j=T_{j\,max}$ T_j= 25 °C	$V_D=V_{DRM}$; $V_R=V_{RRM}$
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage1), min	V/μs	1000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.50 2.00 1.50	$T_j= T_{j\,min}$ T_j=25 °C $T_j= T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	250 150 100	$T_j= T_{j\,min}$ T_j= 25 °C $T_j= T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time, max	μs	3.00	T_j=25 °C; V_D=1500 V; $I_{TM}=I_{TAV}$; di/dt=200 A/μs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 μs; di_G/dt=2 A/μs	
t_q	Turn-off time2), max	μs	400	dv_D/dt=50 V/μs; $T_j=T_{j\,max}$; I_{TM}=160 A; di_R/dt=-10 A/μs; V_R=100V; V_D=0.67 V_{DRM}	
Q_{rr}	Total recovered charge, max	μC	1050	$T_j=T_{j\,max}$; I_{TM}=150 A; di_R/dt=-5 A/μs; V_R=100 V	
t_{rr}	Reverse recovery time, max	μs	30		
I_{rr}	Reverse recovery current, max	A	70		
THERMAL					
R_{thjc}	Thermal resistance, junction to case			180° half-sine wave, 50 Hz	
	per module	°C/W	0.0550		
	per arm	°C/W	0.1100		
R_{thch}	Thermal resistance, case to heatsink				
	per module	°C/W	0.0200		
	per arm	°C/W	0.0400		
INSULATION					
V_{ISOL}	Insulation test voltage	kV	3.00	Sine wave, 50 Hz; RMS	t=60 sec
			3.60		t=1 sec
MECHANICAL					
M_1	Mounting torque (M6)3)	Nm	6.00	Tolerance ± 15%	
M_2	Terminal connection torque (M8)3)	Nm	9.00	Tolerance ± 15%	
m	Weight, max	g	860		

PART NUMBERING GUIDE

MT	3	-	160	-	36	-	A2	H2	-	C1	-	N
1	2		3		4		5	6		7		8

1. Thyristor module (MT)
   Thyristor – Diode module (MT/D)
   Diode – Thyristor module (MD/T)
2. Circuit Schematic
3. Average On-state Current, A
4. Voltage Code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time ($dv_D/dt=50$ V/μs)
7. Package Type (M.C1)
8. Ambient Conditions:
   N – Normal

NOTES

[1] Critical rate of rise of off-state voltage

Symbol of group	A2
$(dv_D/dt)_{crit}$, V/μs	1000

[2] Turn-off time ($dv_D/dt=50$ V/μs)

Symbol of group	H2
t_q, μs	400

[3] The screws must be lubricated

UL certified file-No. E255404

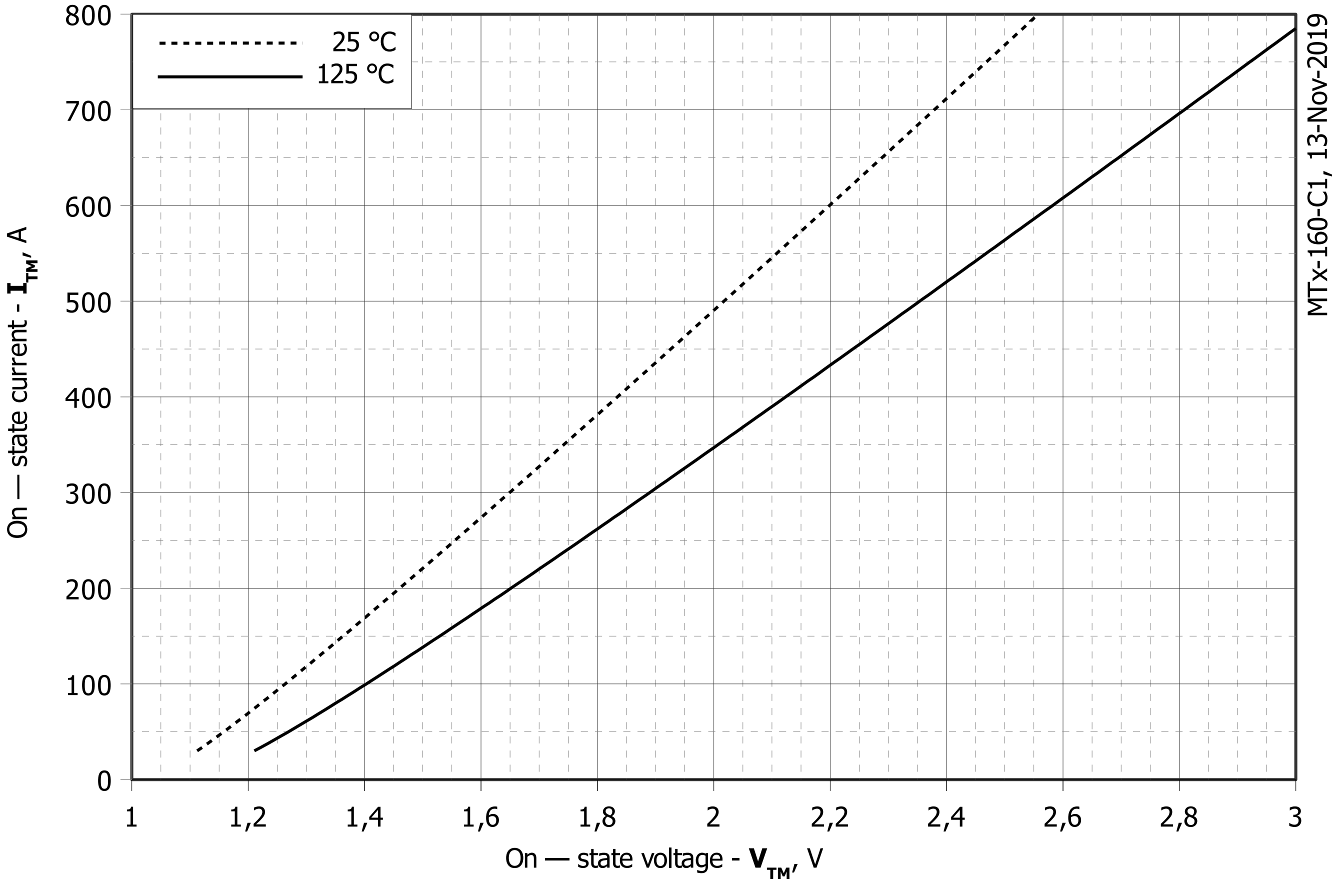


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	$T_j = 25°C$	$T_j = T_{j\,max}$
A	1.0126910	1.0794415
B	0.0016636	0.0020860
C	0.0038420	0.0062181
D	0.0066694	0.0086245

On-state characteristic model (see Fig. 1)

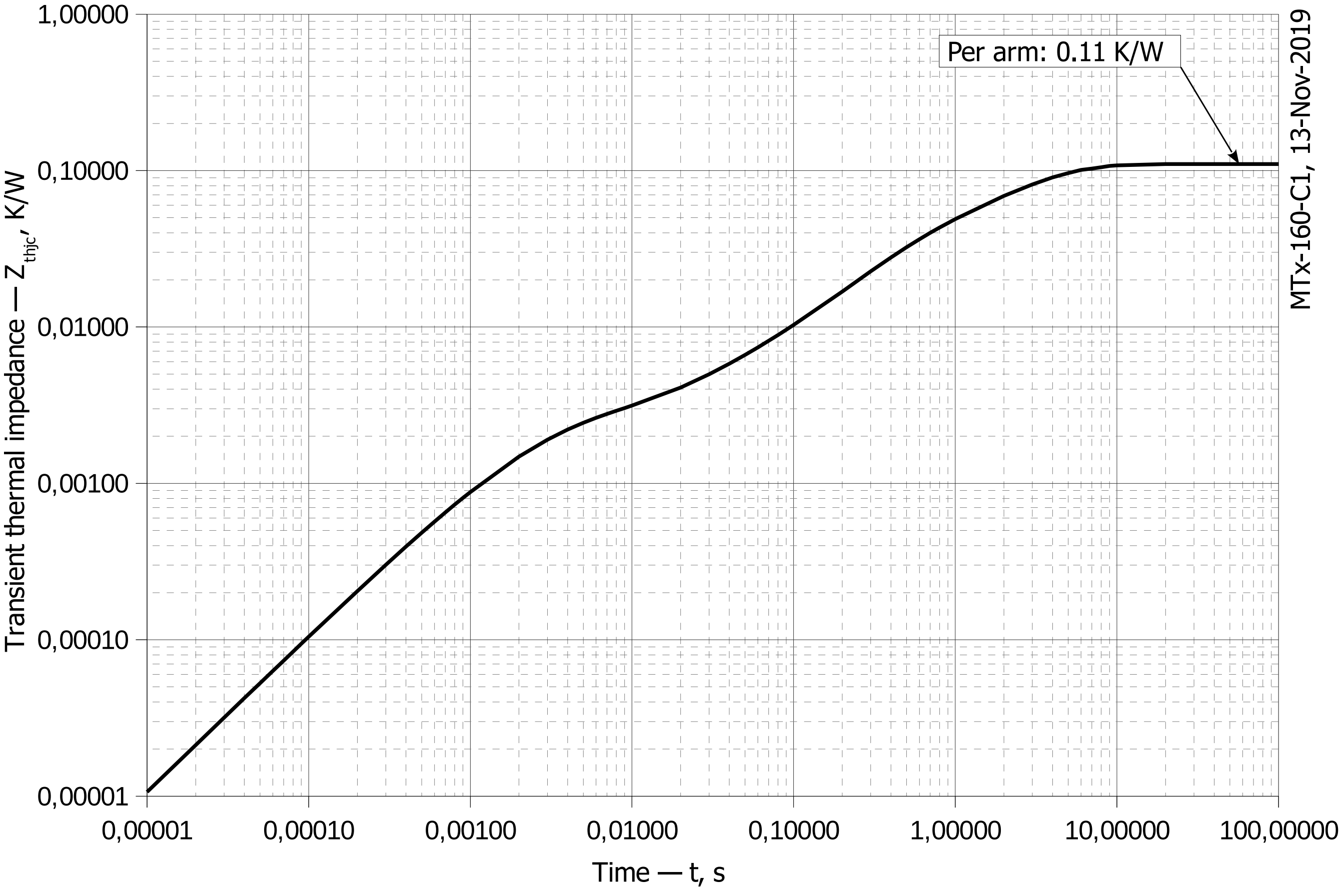


Fig 2 – Transient thermal impedance Z_{thjc} vs. time t

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t.

R_i = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

i	1	2	3	4	5	6
R_i, K/W	0.0808	0.007806	0.02226	-0.007688	0.00471	0.00217
τ_i, s	2.801	1.283	0.3281	0.09408	0.0572	0.002255

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

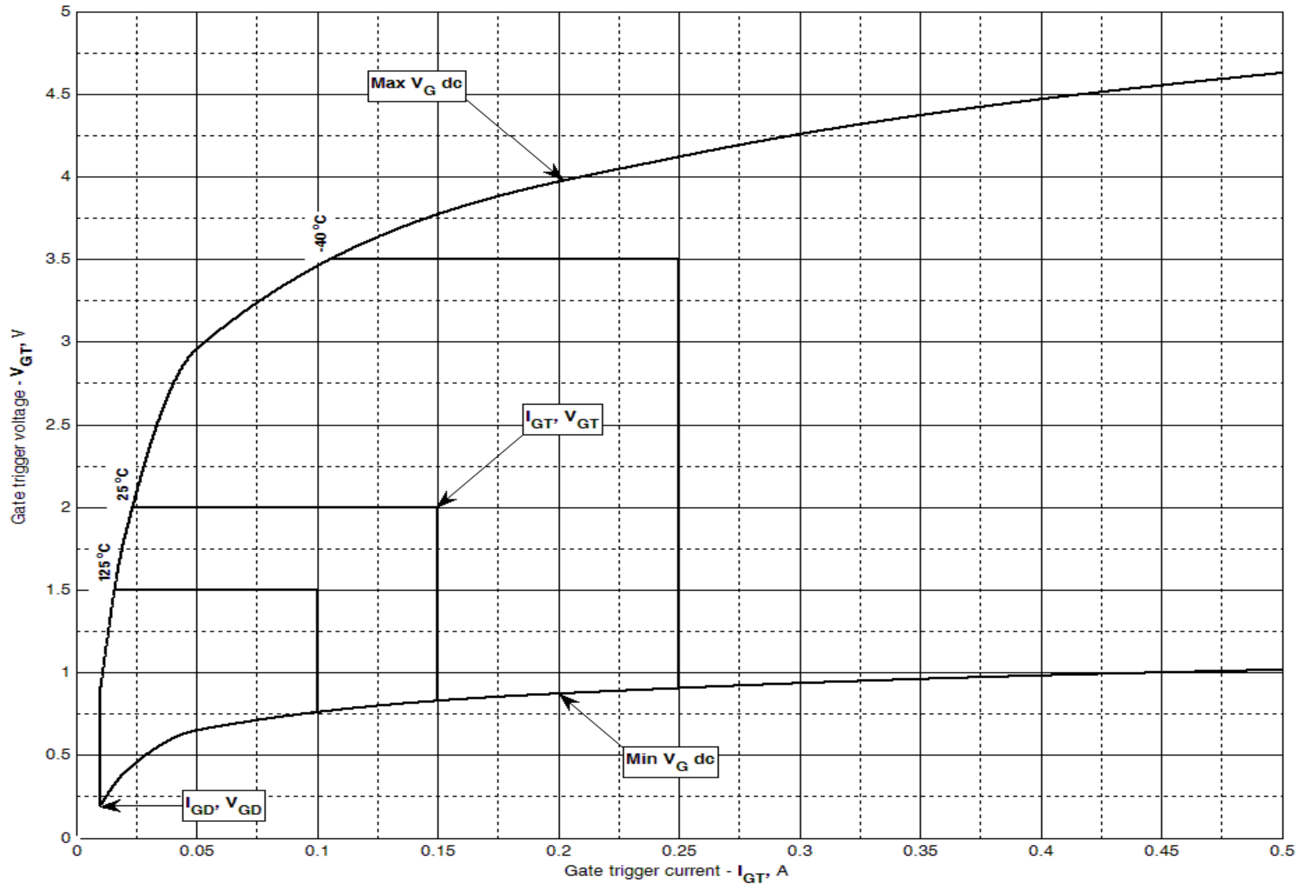


Fig 3 – Gate characteristics – Trigger limits

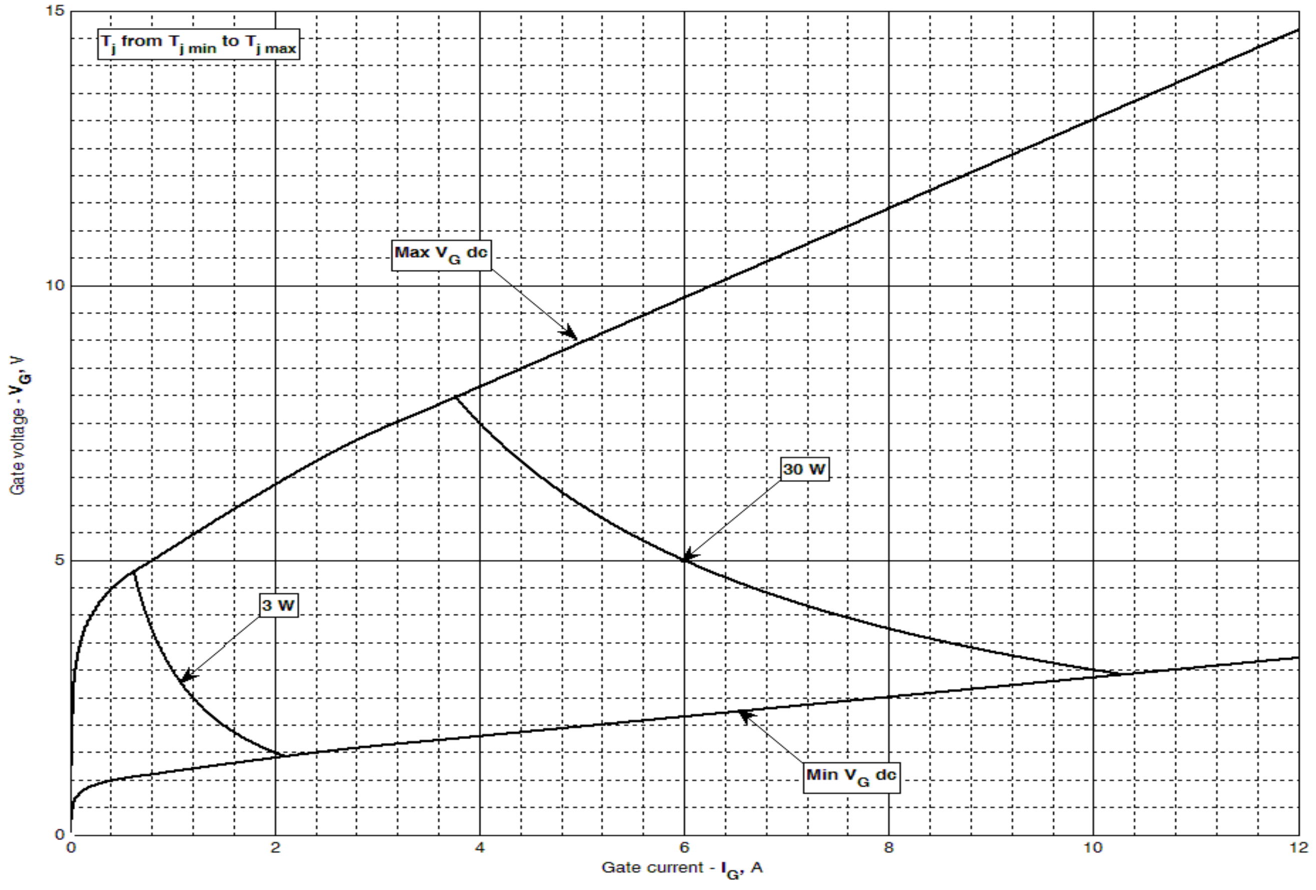


Fig 4 - Gate characteristics – Power curves

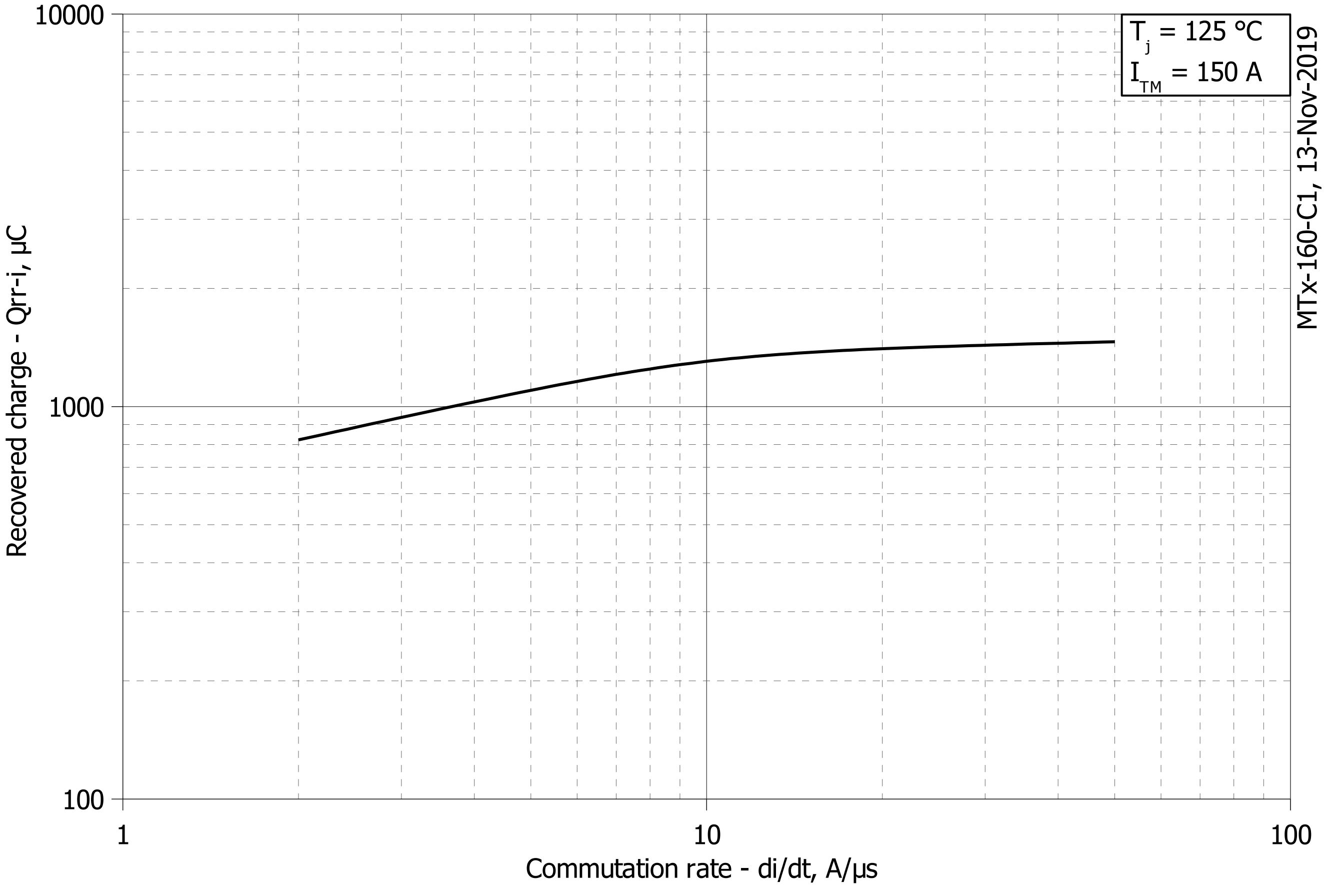


Fig 5 – Maximum recovered charge Q_{rr-i} (integral) vs. commutation rate di_R/dt

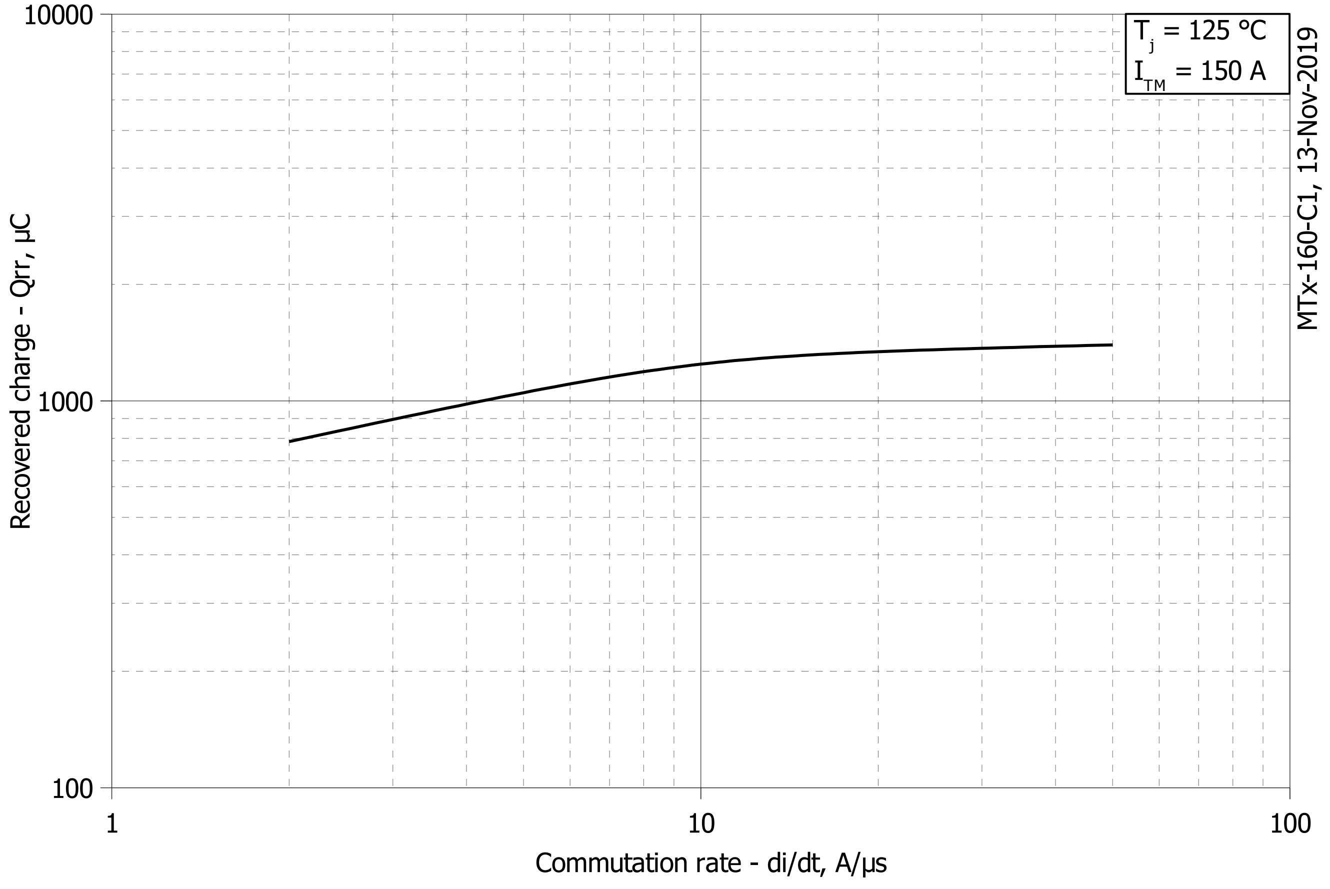


Fig 6 – Maximum recovered charge Q_{rr} vs. commutation rate di_R/dt (25% chord)

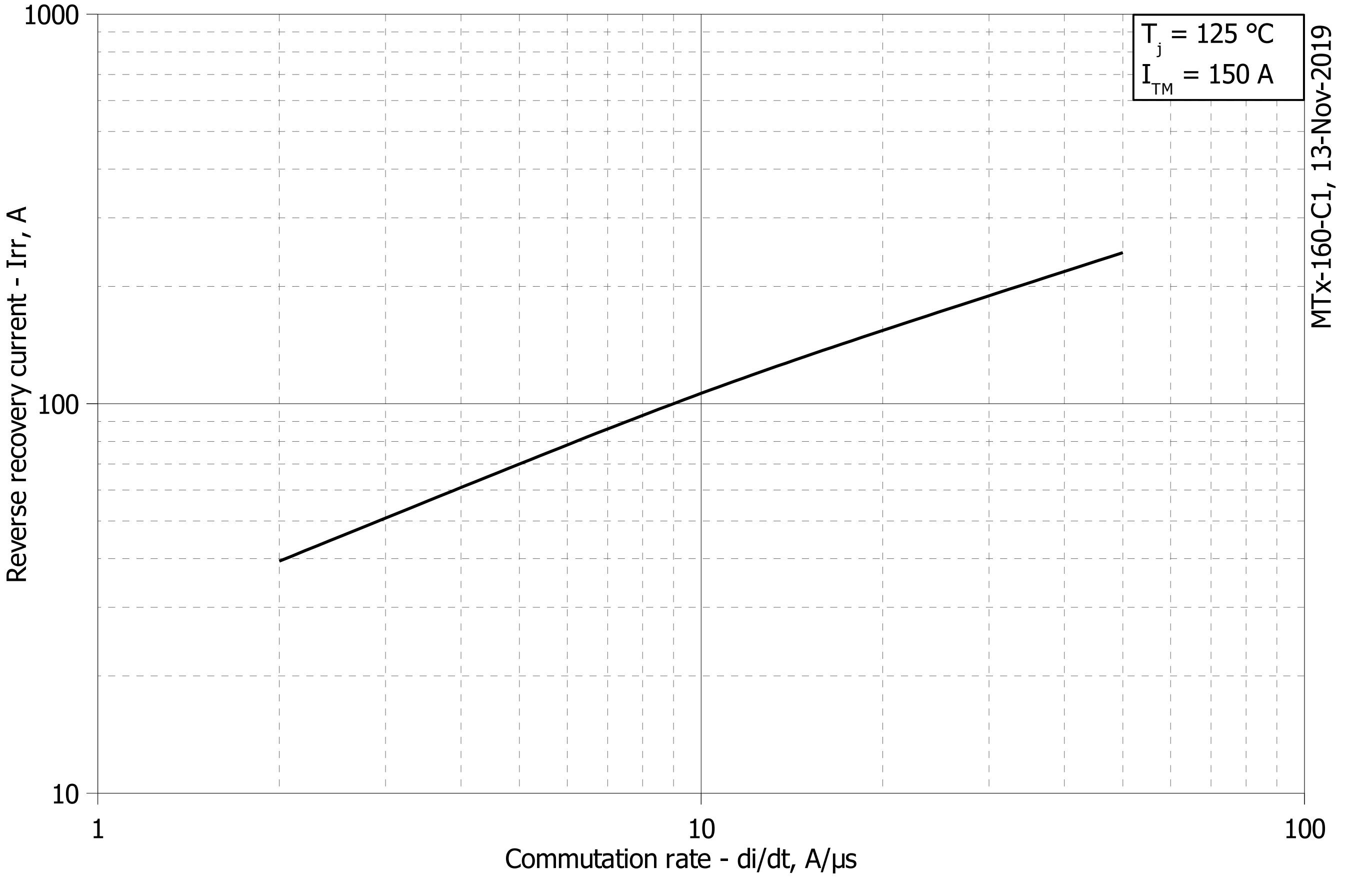


Fig 7 – Maximum reverse recovery current I_{rr} vs. commutation rate di_R/dt

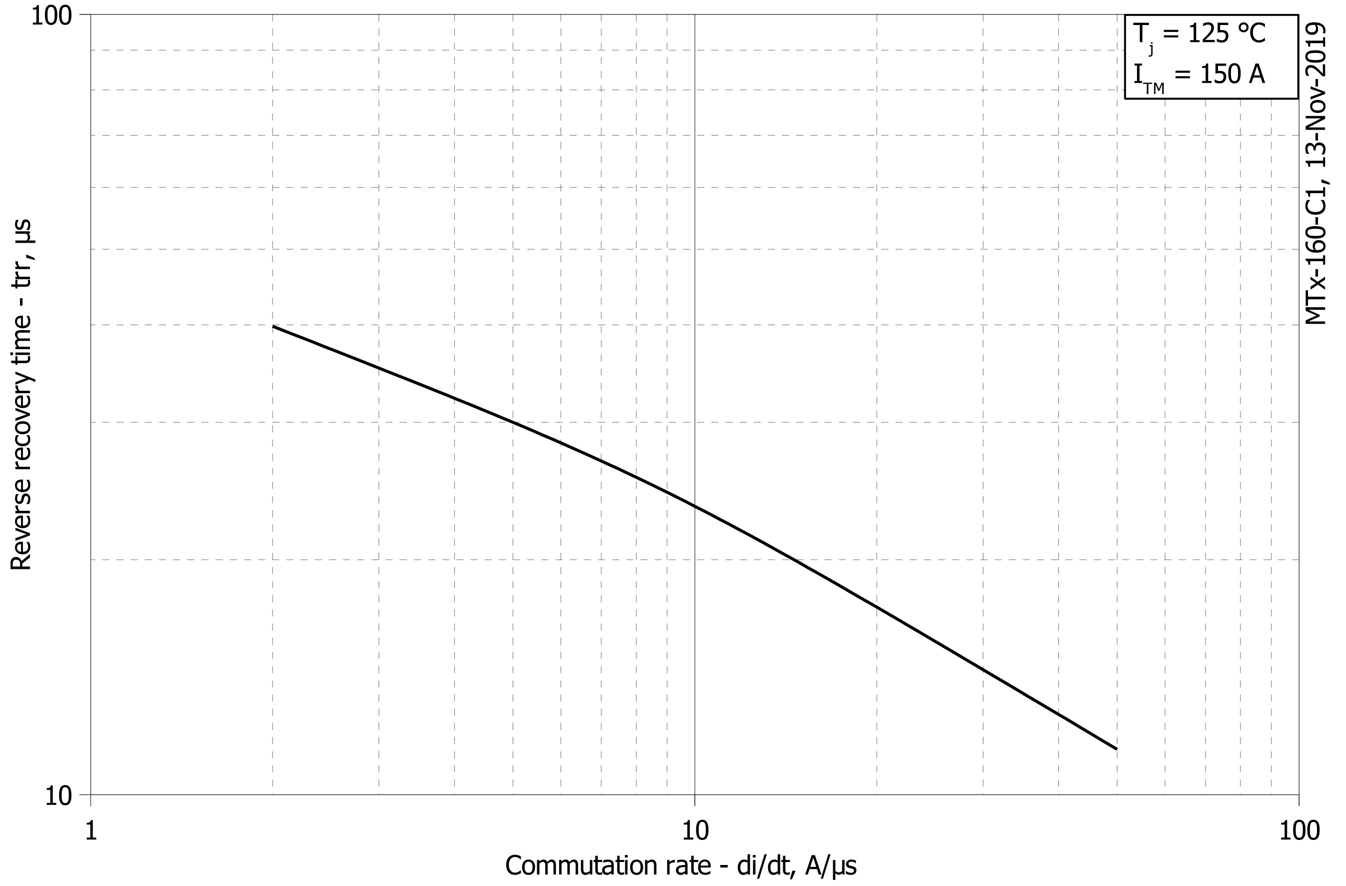


Fig 8 – Maximum recovery time t_{rr} vs. commutation rate di_R/dt (25% chord)

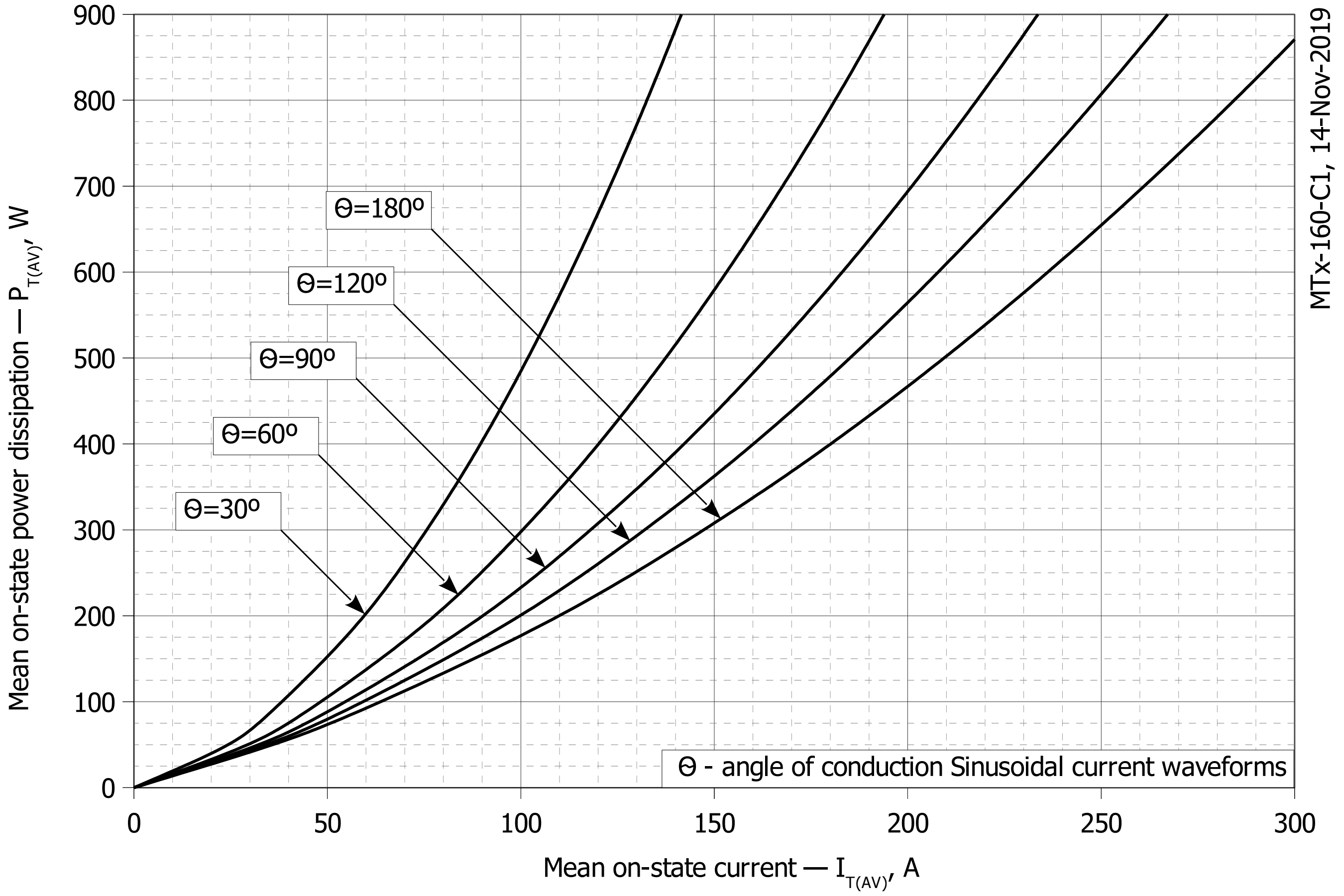


Fig. 9 - Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for sinusoidal current waveforms at different conduction angles (f=50Hz, DSC)

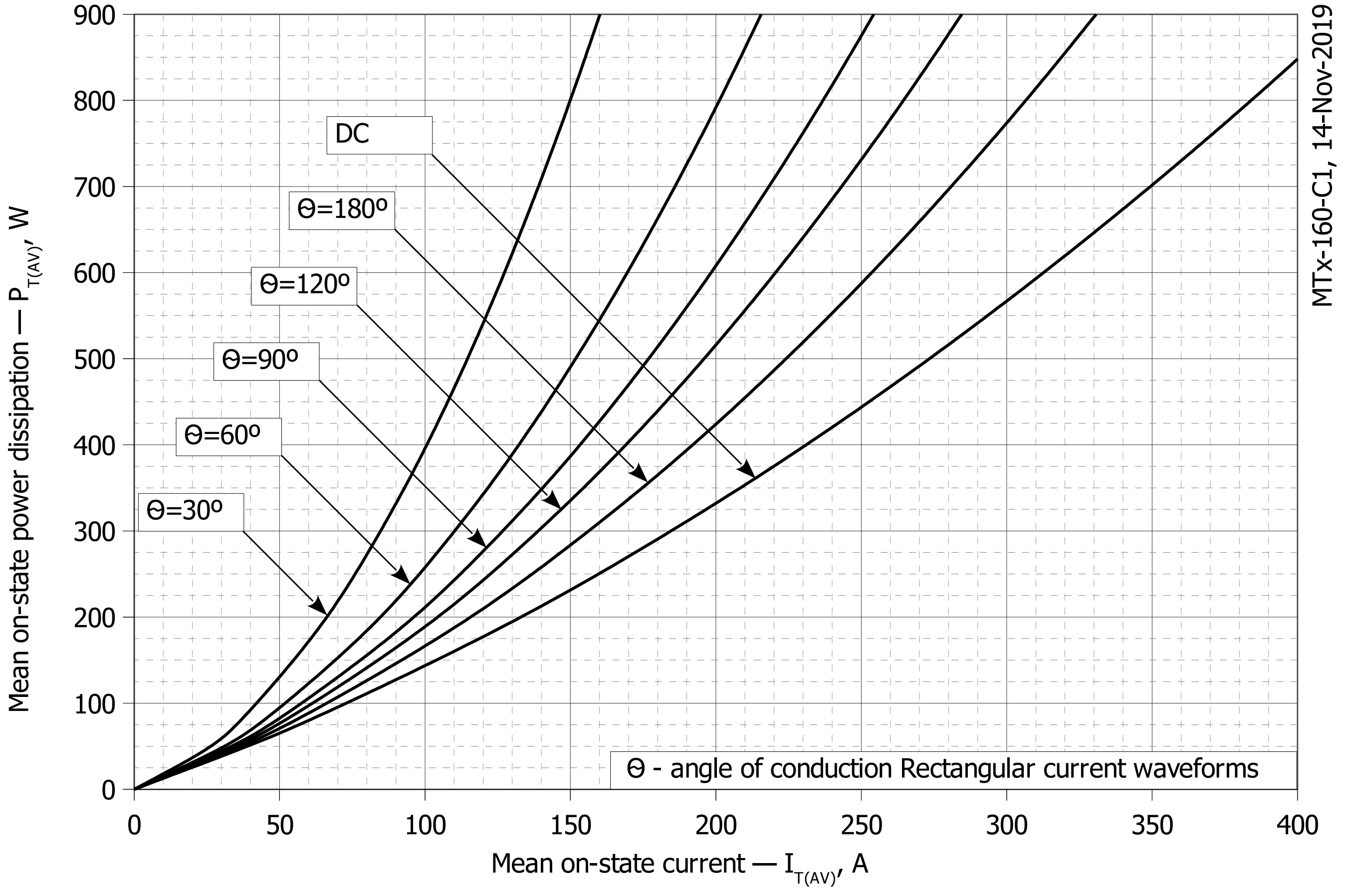


Fig. 10 – Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for rectangular current waveforms at different conduction angles and for DC (f=50Hz, DSC)

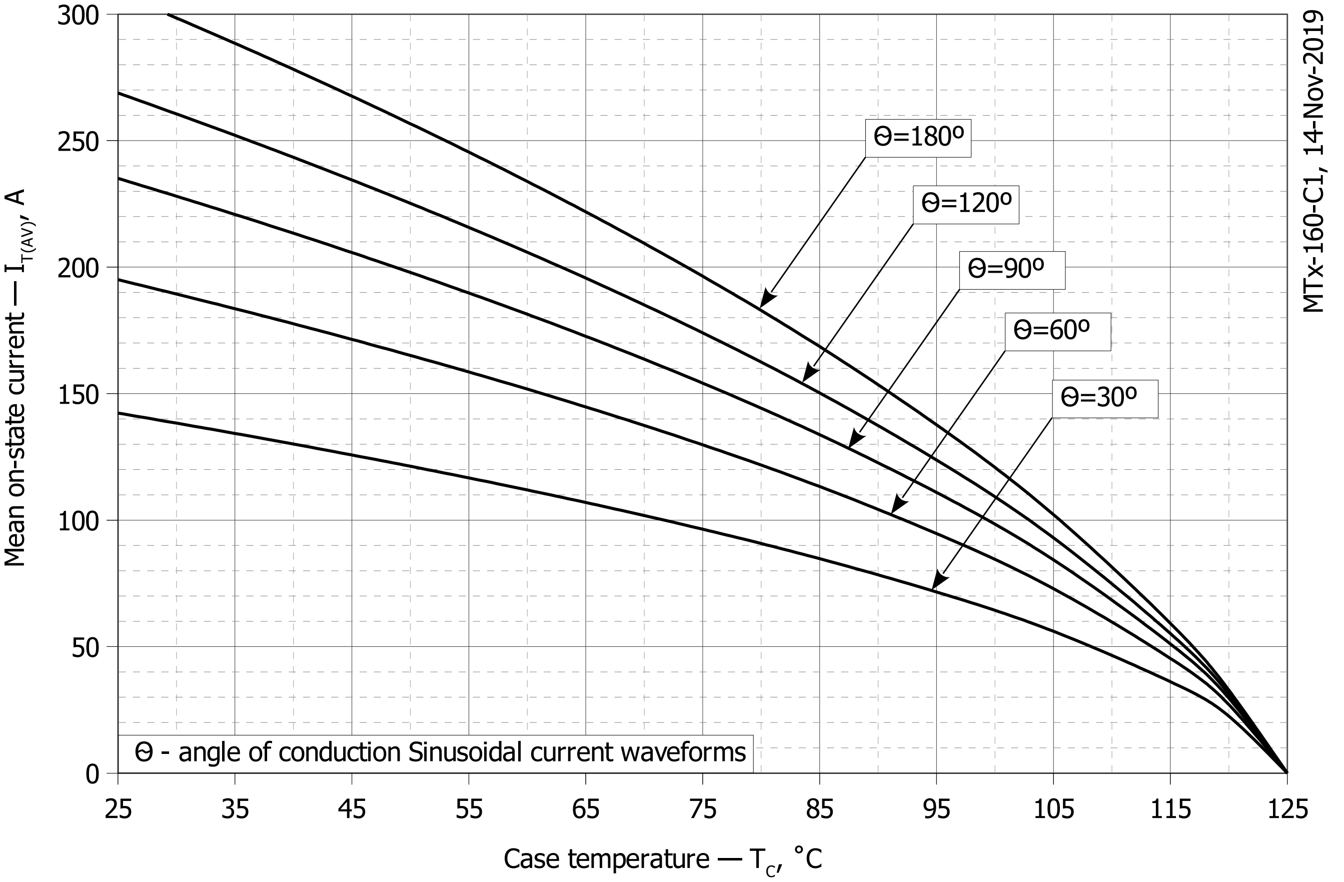


Fig. 11 – Mean on-state current I_{TAV} vs. case temperature T_C for sinusoidal current waveforms at different conduction angles (f=50Hz, DSC)

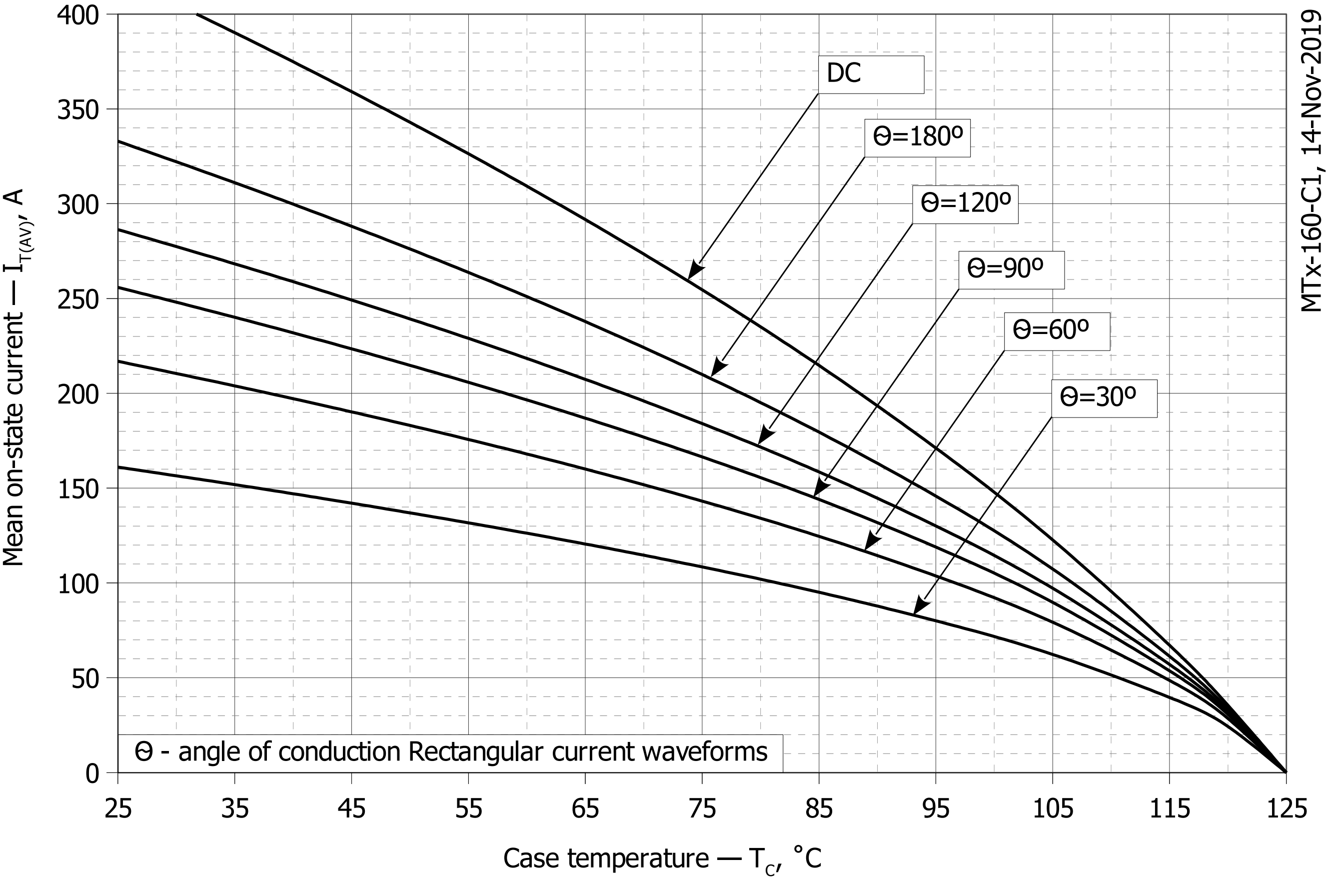


Fig. 12 - Mean on-state current I_{TAV} vs. case temperature T_C for rectangular current waveforms at different conduction angles and for DC (f=50Hz, DSC)

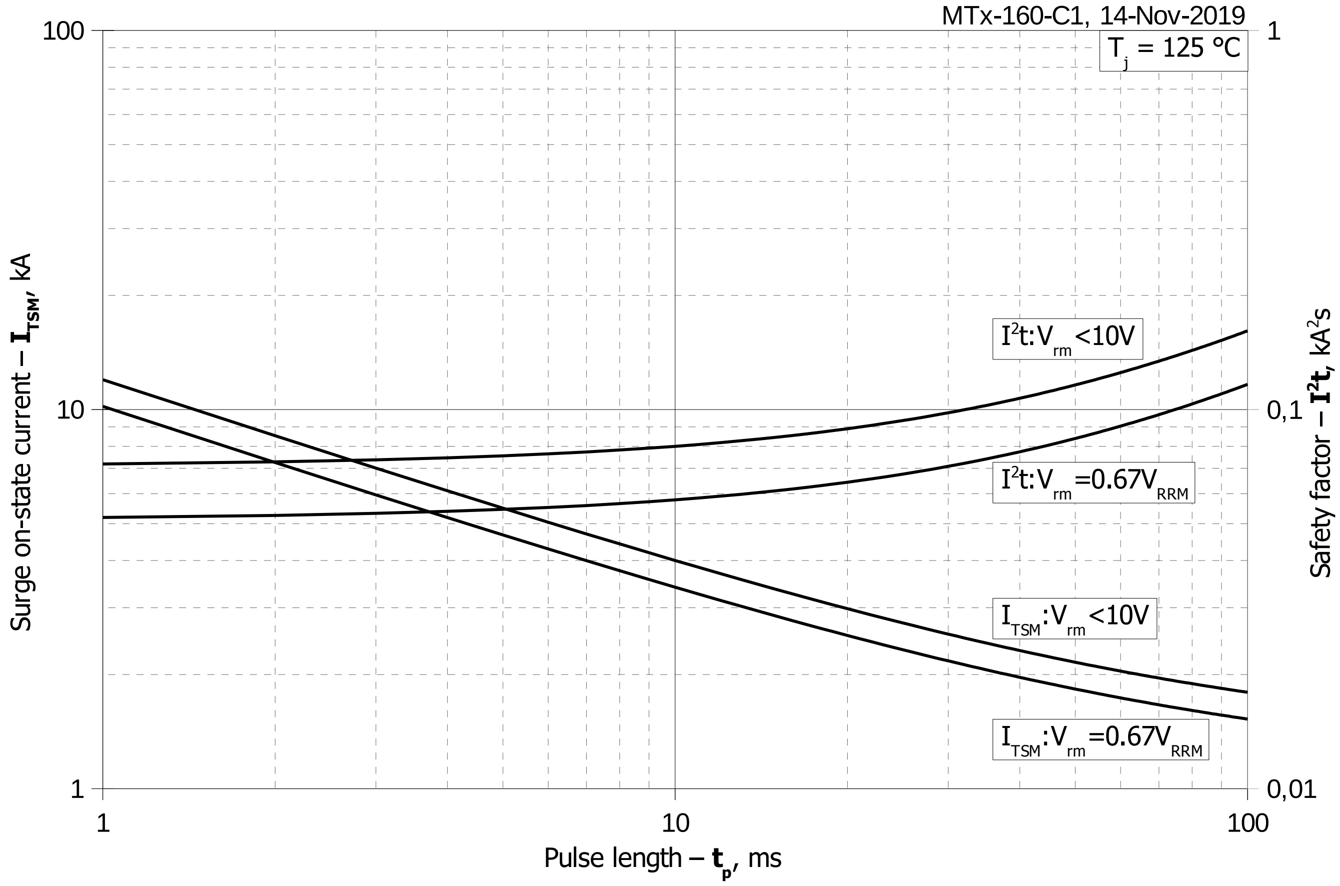


Fig. 13 – Maximum surge on-state current I_{TSM} and safety factor I^2t vs. pulse length t_p

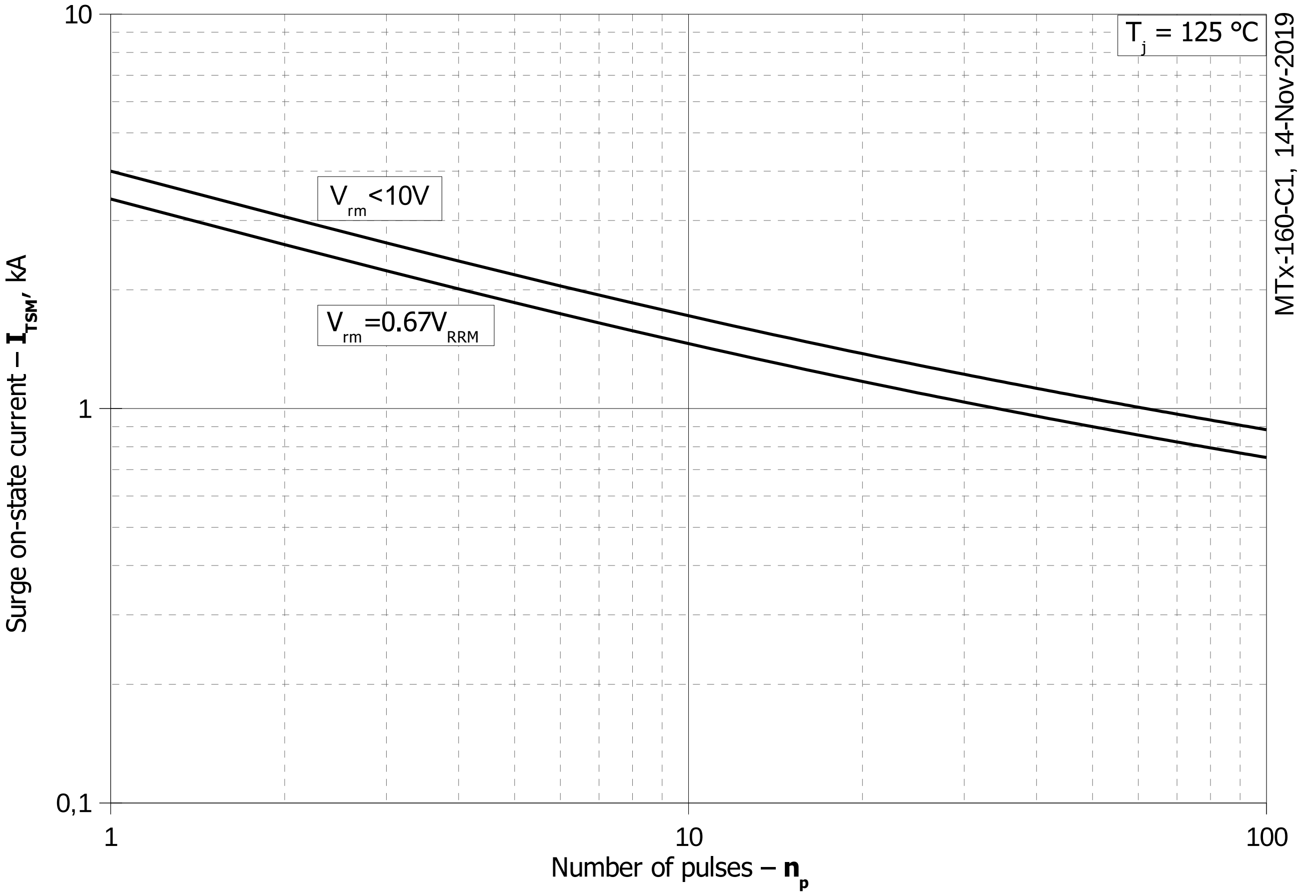


Fig. 14 - Maximum surge on-state current I_{TSM} vs. number of pulses n_p