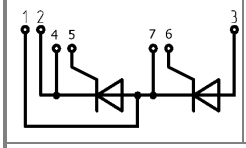
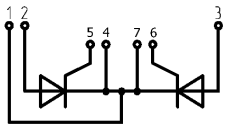
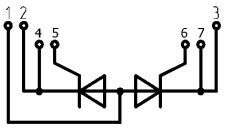
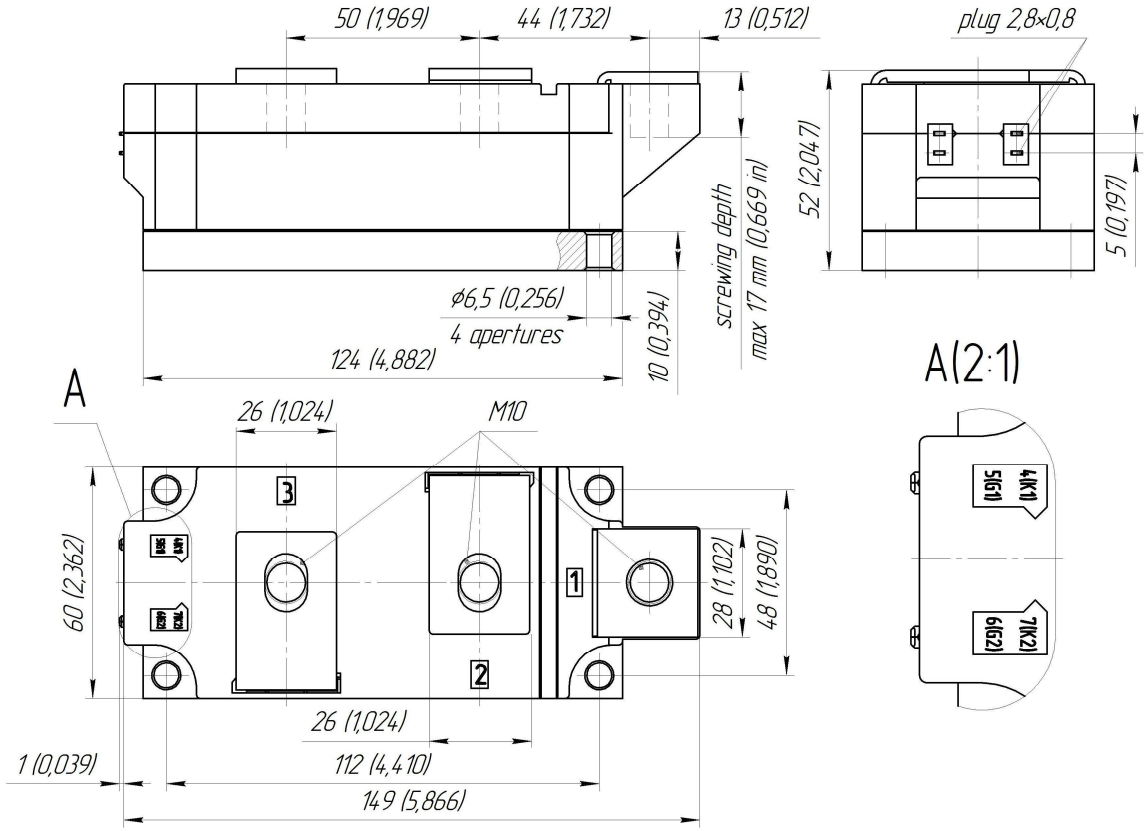
Double Thyristor Module For Phase Control MTx-240-65-A2

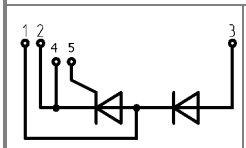
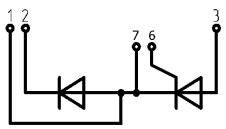
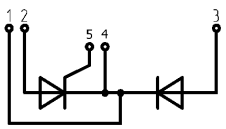
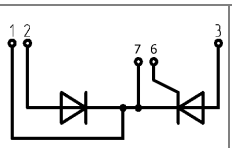
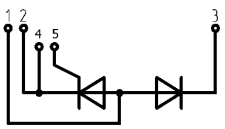
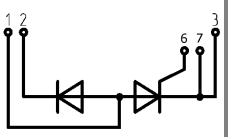
Electrically isolated base plate
Industrial standard package
Simplified mechanical design, rapid assembly
Pressure contact

Mean on-state current	I_{TAV}	240 A
Repetitive peak off-state voltage	V_{DRM}	4600 ÷ 6500 V
Repetitive peak reverse voltage	V_{RRM}	4600 ÷ 6500 V
Turn-off time	t_q	630 µs

V_{DRM}, V_{RRM}, V	4600	4800	5000	5200	5400	5600	5800	6000	6200	6400	6500
Voltage code	46	48	50	52	54	56	58	60	62	64	65
T_j, °C	– 40 ÷ 125										

MT3		MT4		MT5	
					



MT/D3	MD/T3	MT/D4	MD/T4	MT/D5	MD/T5
					

All dimensions in millimeters (inches)

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	240	T_c=85 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	376		
I_{TSM}	Surge on-state current	kA	4.0 4.6	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			4.2 4.8	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	$A^2s\cdot10^3$	80 106	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			73 97	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600÷6500	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700÷6600	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75\cdot V_{DRM}$ $0.75\cdot V_{RRM}$	$T_j=T_{j\,max}$; Gate open	
TRIGGERING					
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\,max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	4	$T_j=T_{j\,max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	500	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
THERMAL					
T_{stg}	Storage temperature	°C	-40 ÷ 125		
T_j	Operating junction temperature	°C	-40 ÷ 125		
MECHANICAL					
a	Acceleration under vibration	m/s^2	50		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.80	T_j=25 °C; I_{TM}=785 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.10	T_j=$T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	2.500		
I_L	Latching current, max	mA	1000	T_j=25 °C; V_D=12 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	150	T_j=$T_{j\,max}$; V_D=V_{DRM}; V_R=V_{RRM}	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage, min	V/µs	1000	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00 2.50 2.00	T_j= $T_{j\,min}$ T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	T_j= $T_{j\,min}$ T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	15.00		
SWITCHING					
t_{gd}	Delay time	µs	3.50	T_j=25 °C; V_D=0.4·V_{DRM}; I_{TM}=I_{TAV}; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
t_q	Turn-off time, max	µs	630	dv_D/dt=50 V/µs; T_j=$T_{j\,max}$; I_{TM}= I_{TAV}; di_R/dt=-10 A/µs; V_R=100V; V_D=0.67 V_{DRM};	
THERMAL					
R_{thjc}	Thermal resistance, junction to case				
	per module	°C/W	0.0340	180° half-sine wave, 50 Hz	
	per arm	°C/W	0.0680		
	per module	°C/W	0.0325	DC	
	per arm	°C/W	0.0650		
R_{thch}	Thermal resistance, case to heatsink				
	per module	°C/W	0.0100		
	per arm	°C/W	0.0200		
INSULATION					
V_{ISOL}	Insulation test voltage	kV	3.00	Sine wave, 50 Hz; RMS	t=1 min
			3.60		t=1 sec
MECHANICAL					
M_1	Mounting torque (M6)[1)]	Nm	6.00	Tolerance ± 15%	
M_2	Terminal connection torque (M10)[1)]	Nm	12.00	Tolerance ± 15%	
w	Weight	g	1500		

PART NUMBERING GUIDE	NOTES
MT 3 - 240 - 65 - A2 - N 1 2 3 4 5 6 1. Thyristor module (MT) Thyristor – Diode module (MT/D) Diode – Thyristor module (MD/T) 2. Circuit Schematic: 3 – serial connection 4 – common Cathode 5 – common Anode 3. Average On-state Current, A 4. Voltage Code 5. Package Type (M.A2) 6. Ambient Conditions: N – Normal	[1] The screws must be lubricated
UL certified file-No. E255404	