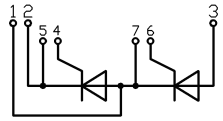
Double Thyristor Module For Phase Control MTx-165-22-F

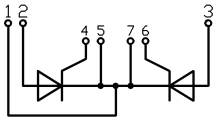
Electrically isolated base plate
Industrial standard package
Simplified mechanical design, rapid assembly
Pressure contact

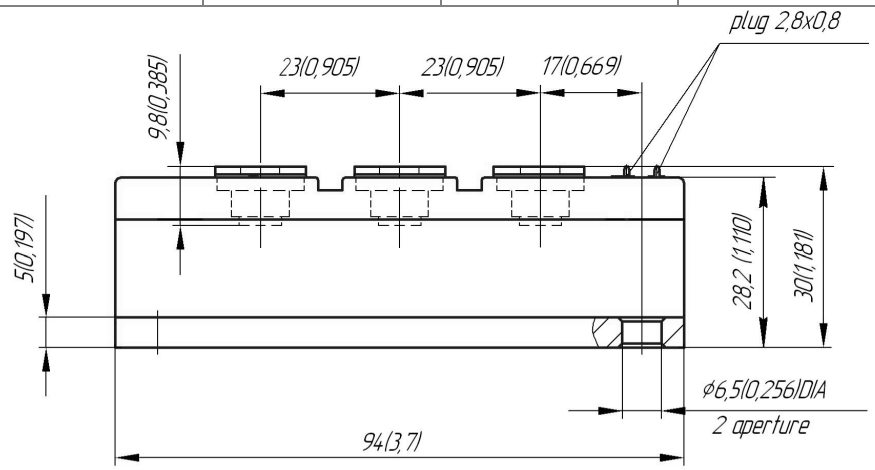
Mean on-state current		I_{TAV}	165 A
Repetitive peak off-state voltage		V_{DRM}	2000 ÷ 2200 V
Repetitive peak reverse voltage		V_{RRM}	
Turn-off time		t_q	125 µs
V_{DRM}, V_{RRM}, V	2000		2200
Voltage code	20		22
T_j, °C	– 40 ÷ 125		

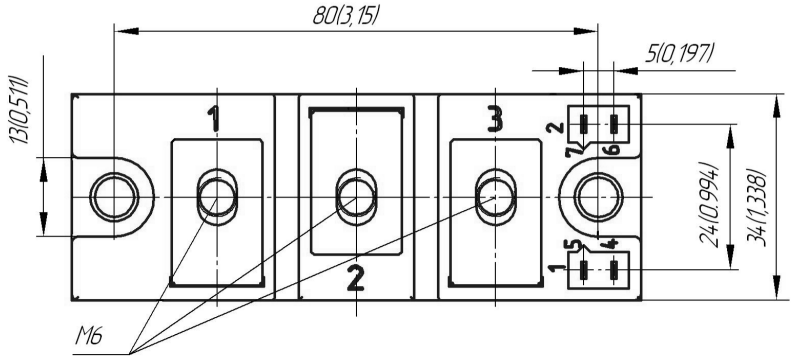
MT3

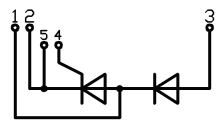


MT4

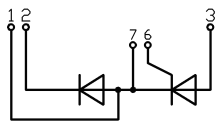




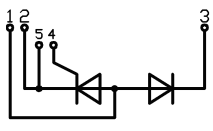




MT/D3



MD/T3



MT/D5

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	165	T_c= 85 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	259		
I_{TSM}	Surge on-state current	kA	4.7 5.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			5.0 5.8	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	$A^2s\cdot10^3$	110 145	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			100 135	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000÷2200	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100÷2300	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open	
TRIGGERING					
I_{FGM}	Peak forward gate current	A	5	T_j=$T_{j\,max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	3	T_j=$T_{j\,max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	500	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; I_{TM}=2 I_{TAV}; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
THERMAL					
T_{stg}	Storage temperature	°C	-40 ÷ 125		
T_j	Operating junction temperature	°C	-40 ÷ 125		
MECHANICAL					
a	Acceleration under vibration	m/s^2	50		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.50	T_j=25 °C; I_{TM}= 500 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.80	$T_j=T_{j\,max}$; $0.5\,\pi\,I_{TAV} < I_T < 1.5\,\pi\,I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	1.350		
I_L	Latching current, max	mA	500	T_j=25 °C; V_D=12 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
I_H	Holding current, max	mA	250	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	30	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage, min	V/µs	1000	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00 2.50 2.00	T_j= $T_{j\,min}$ T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 250 200	T_j= $T_{j\,min}$ T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time	µs	2.50	T_j=25 °C; $V_D=0.4\cdot V_{DRM}$; $I_{TM}=I_{TAV}$; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
t_q	Turn-off time, max	µs	125	dv_D/dt=50 V/µs; $T_j=T_{j\,max}$; I_{TM}=200 A; di_R/dt=-10 A/µs; V_R=100V; V_D=0.67 V_{DRM};	
Q_{rr}	Total recovered charge, max	µC	855	$T_j=T_{j\,max}$; I_{TM}= 200 A ; di_R/dt=-10 A/µs ; V_R=100 V	
t_{rr}	Reverse recovery time, max	µs	18		
I_{rrM}	Peak reverse recovery current, max	A	95		
THERMAL					
R_{thjc}	Thermal resistance, junction to case				
	per module	°C/W	0.0900	180° half-sine wave, 50 Hz	
	per arm	°C/W	0.1800		
	per module	°C/W	0.0850	DC	
	per arm	°C/W	0.1700		
R_{thch}	Thermal resistance, case to heatsink				
	per module	°C/W	0.0300		
	per arm	°C/W	0.0600		
INSULATION					
V_{ISOL}	Insulation test voltage	kV	3.00	Sine wave, 50 Hz; RMS	t=1 min
			3.60		t=1 sec
MECHANICAL					
M_1	Mounting torque (M6)[1)]	Nm	6.00	Tolerance ± 15%	
M_2	Terminal connection torque (M6)[1)]	Nm	6.00	Tolerance ± 15%	
w	Weight	g	320		

PART NUMBERING GUIDE	NOTES
MT 3 - 165 - 22 - F - N 1 2 3 4 5 6 1. Thyristor module (MT) Thyristor – Diode module (MT/D) Diode – Thyristor module (MD/T) 2. Circuit Schematic 3. Average On-state Current, A 4. Voltage Code 5. Package Type (M.F) 6. Ambient Conditions: N – Normal	[1)] The screws must be lubricated
	UL certified file-No. E255404

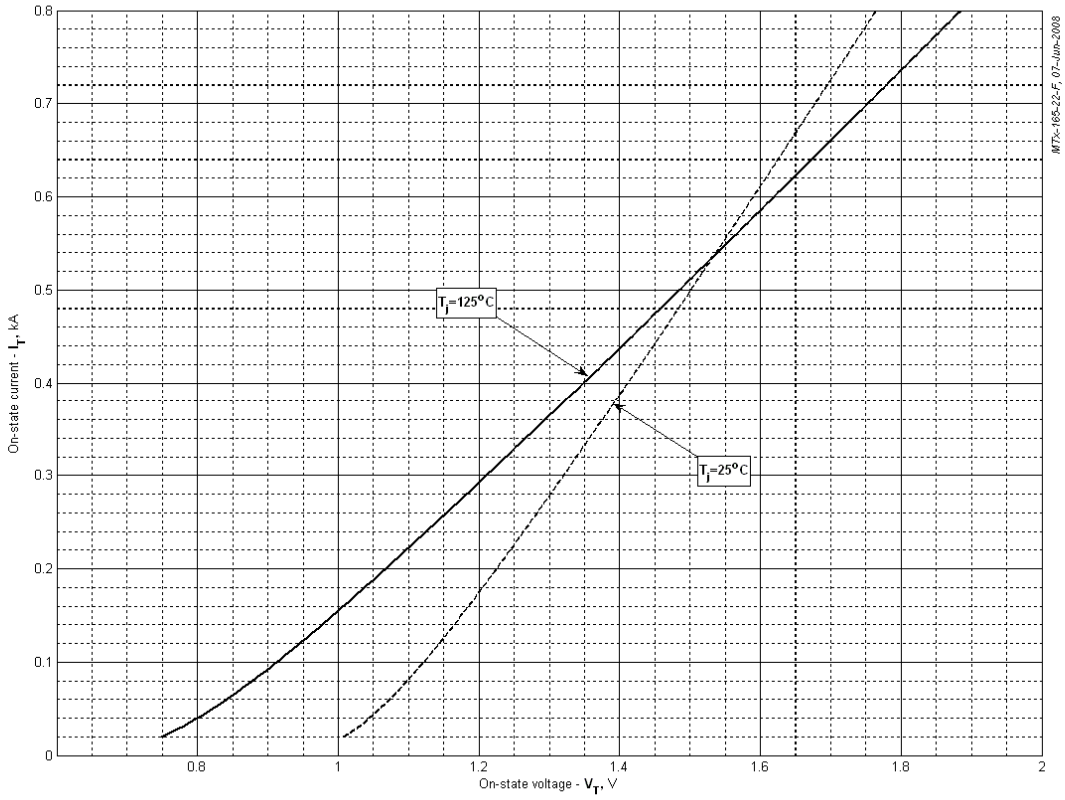


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	T_j = $T_{j\,max}$
A	0.943585	0.659211
B	0.891706	1.352412
C	-0.442302	-0.590725
D	0.411509	0.549600

On-state characteristic model (see Fig. 1)

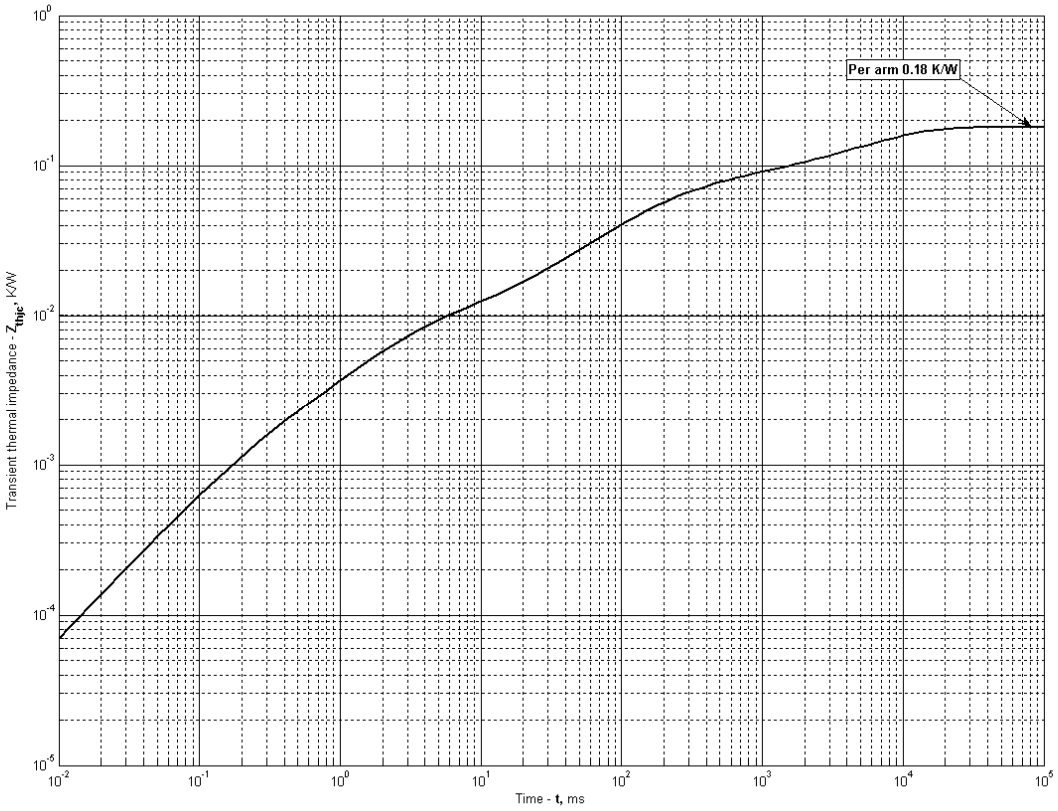


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

$\boldsymbol{\tau_i}$ = Time constatnt of r_{th} term.

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.0007653	0.00703	0.01629	0.04126	0.01513	0.09951
$\boldsymbol{\tau_i}$, **s**	0.0002111	0.002366	0.06905	0.1909	0.6646	6.64

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

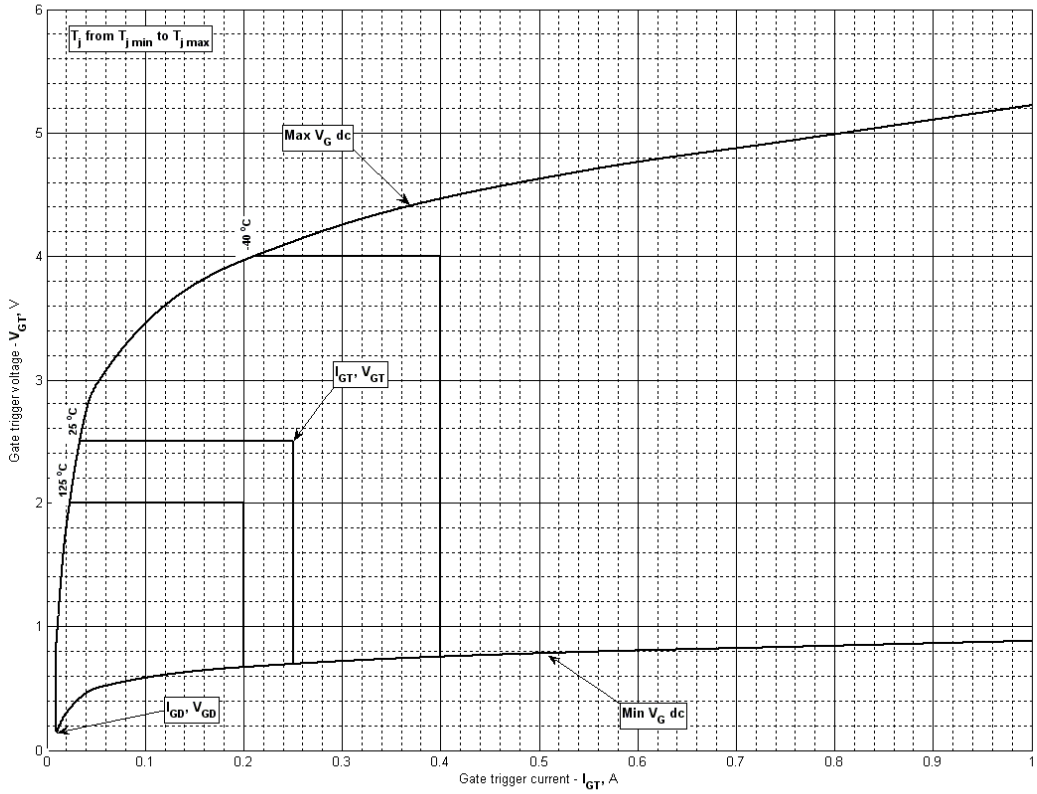


Fig 3 – Gate characteristics – Trigger limits

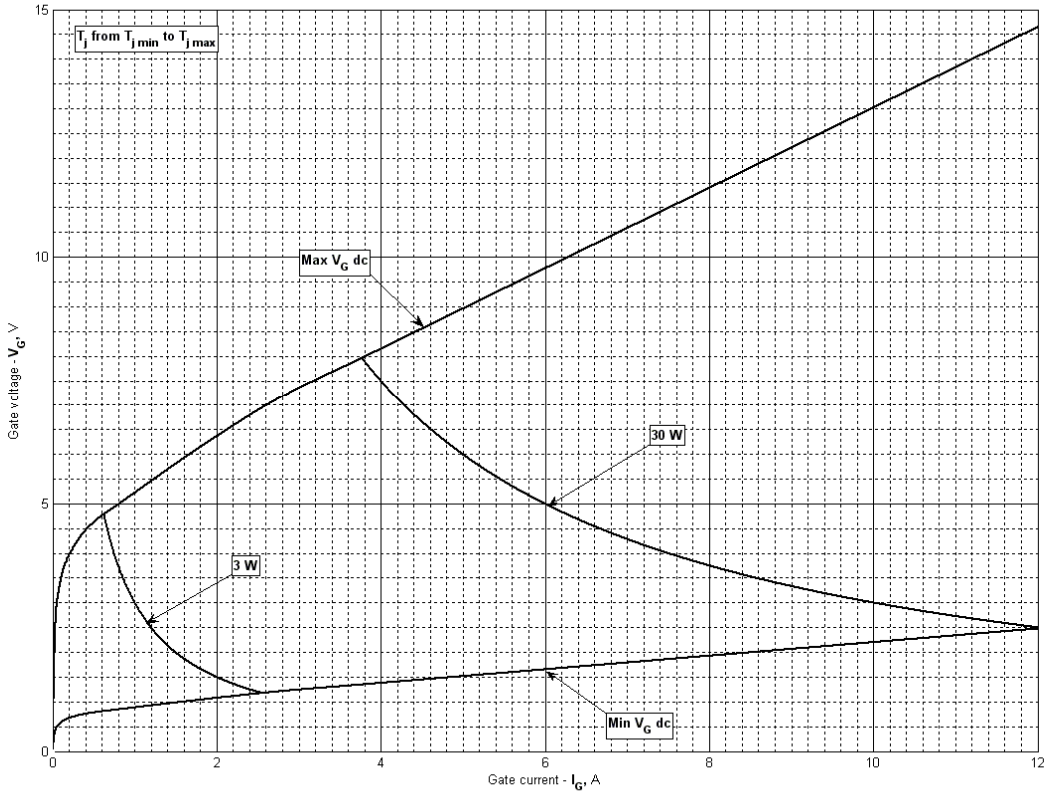


Fig 4 - Gate characteristics – Power curves

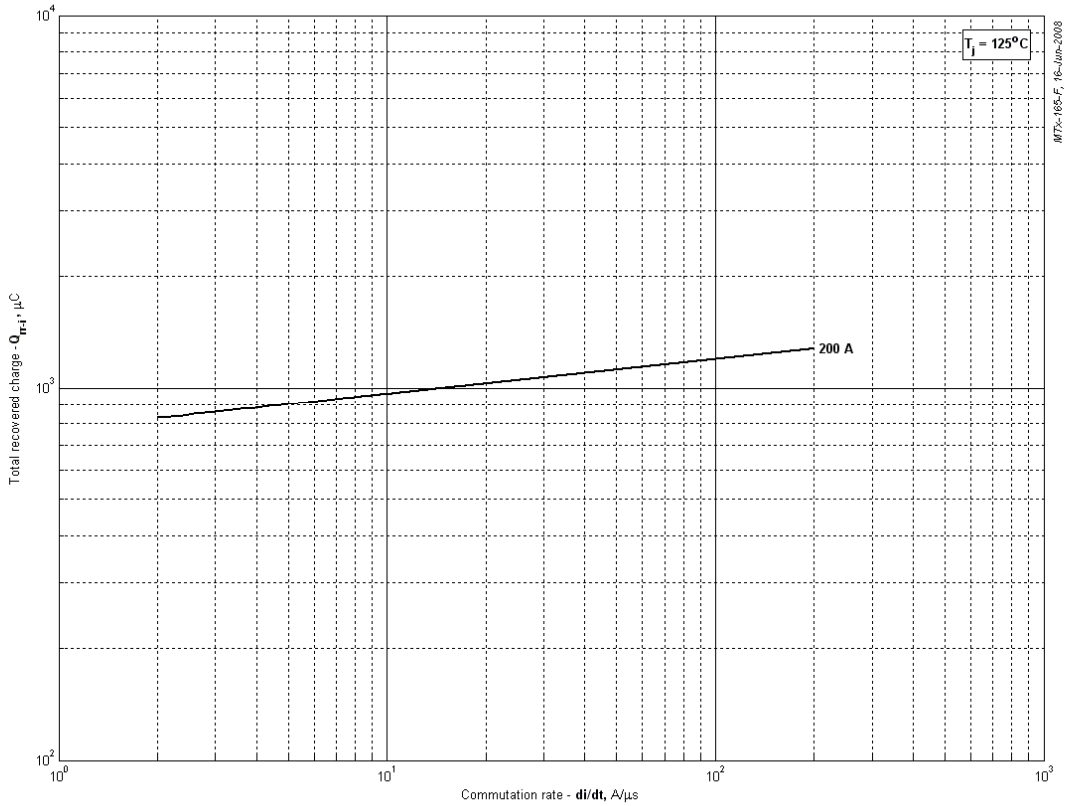


Fig 5 - Total recovered charge, Q_{rr-i} (integral)

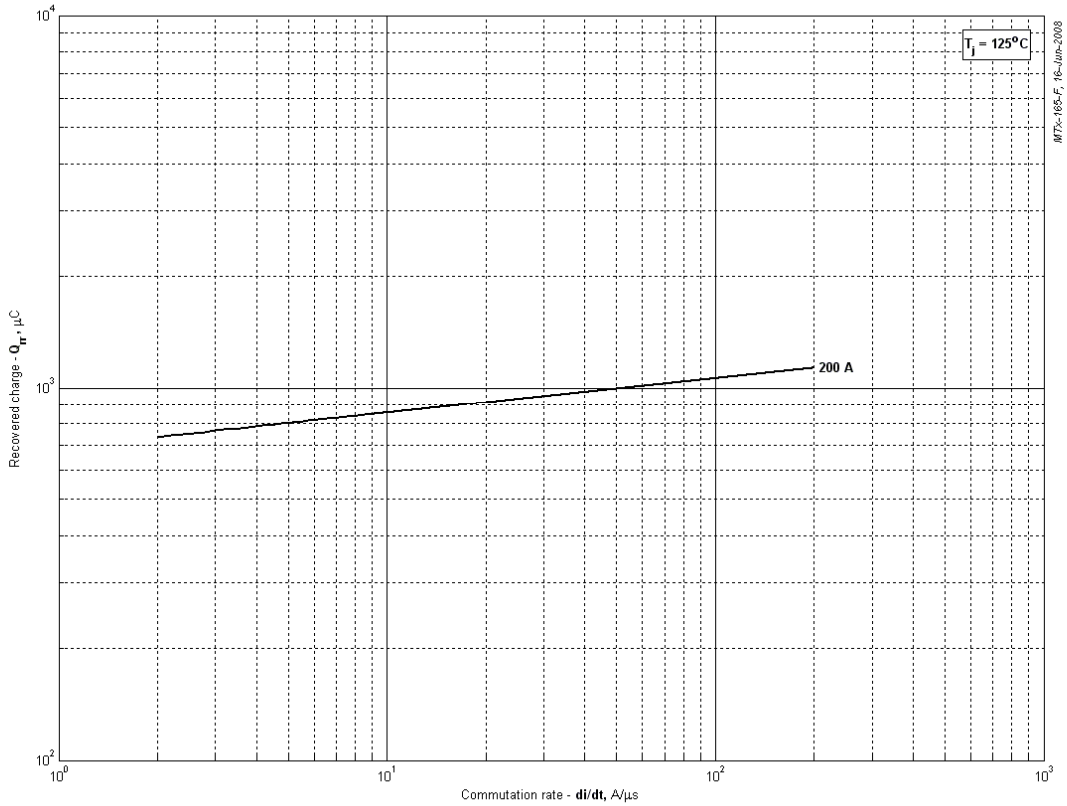


Fig 6 - Recovered charge, Q_{rr} (linear)

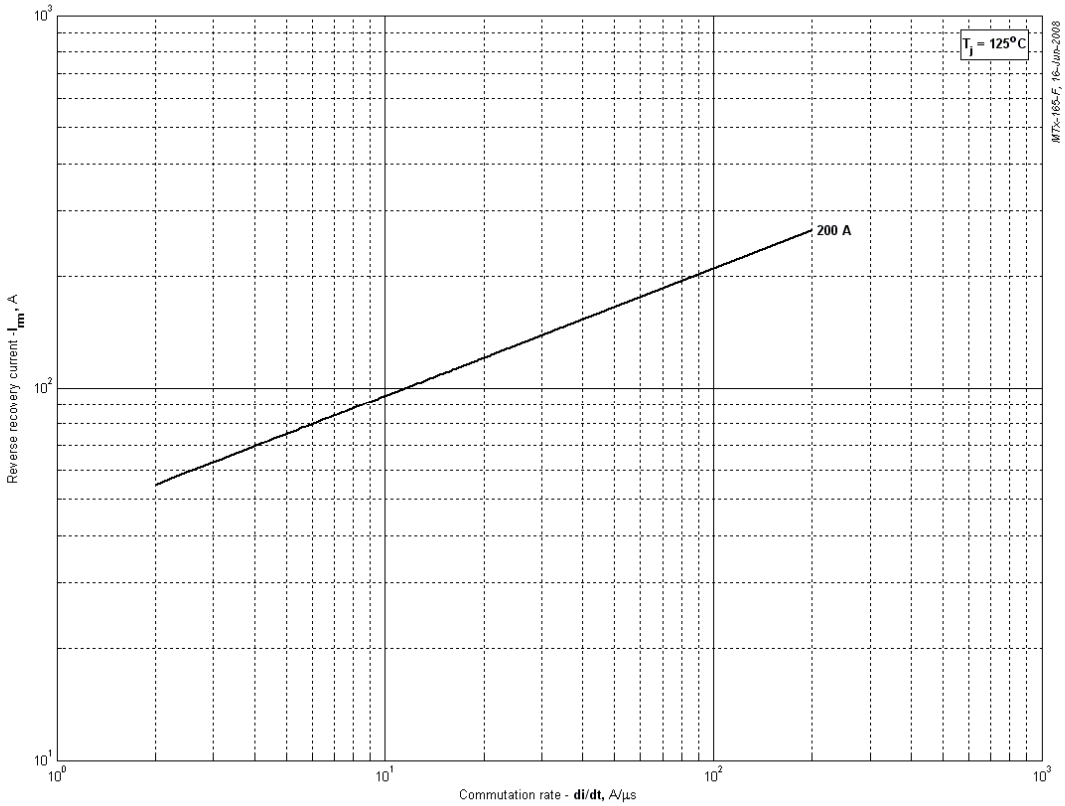


Fig 7 - Peak reverse recovery current, I_{rm}

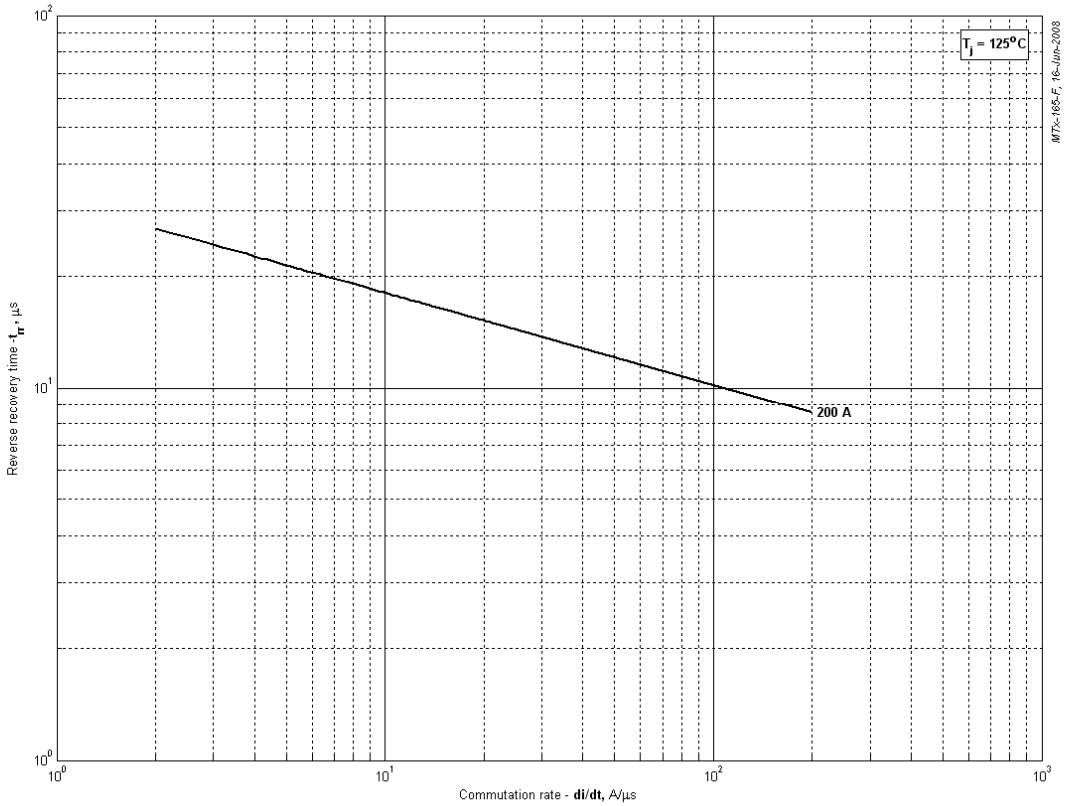


Fig 8 - Recovery time, t_{rr} (50% chord)

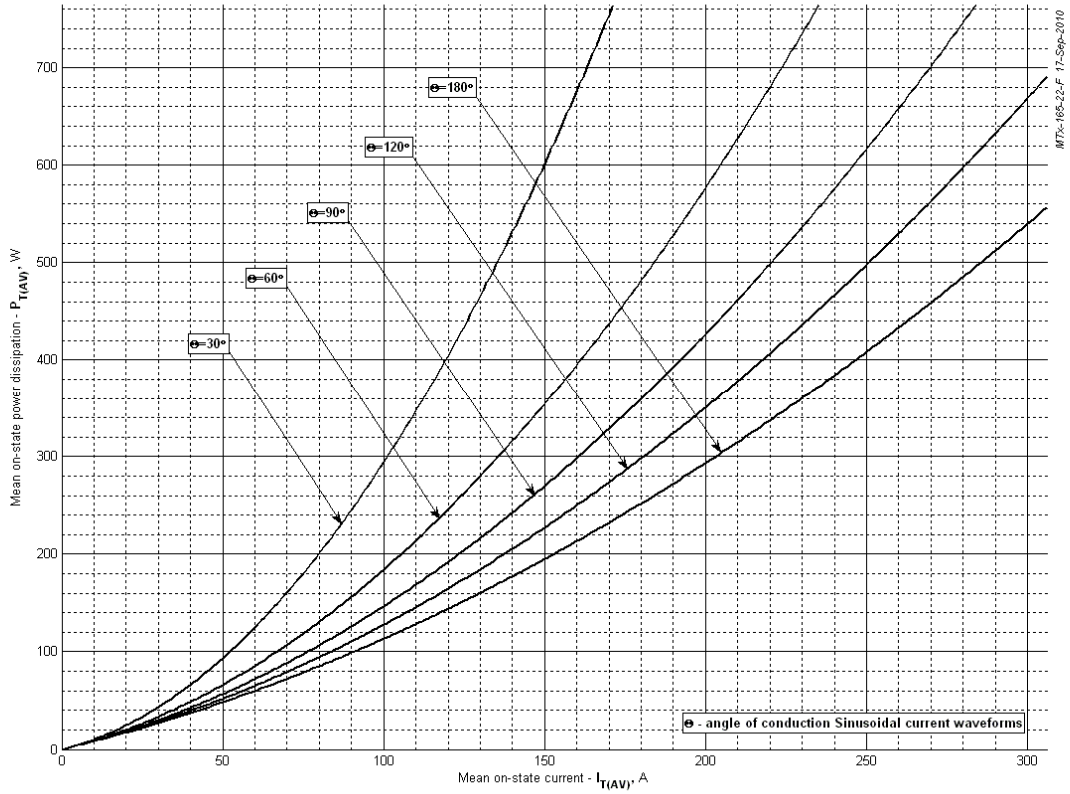


Fig 9 – On-state power loss (sinusoidal current waveforms)

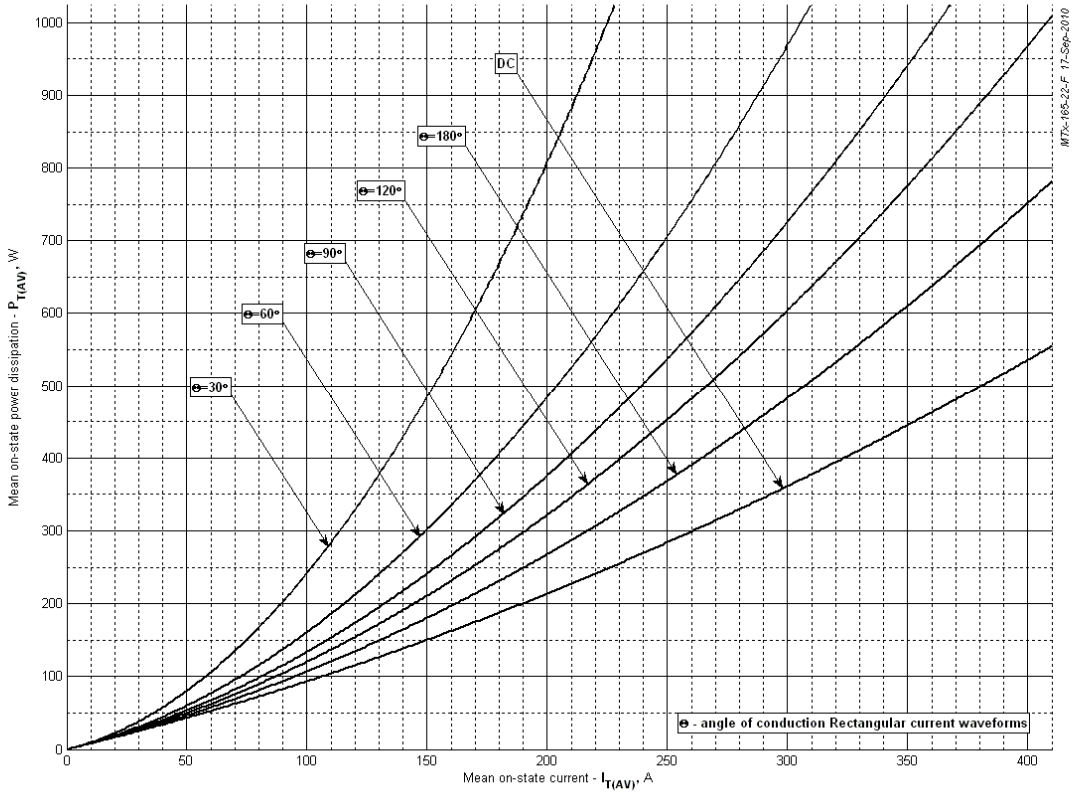


Fig 10 - On-state power loss (rectangular current waveforms)

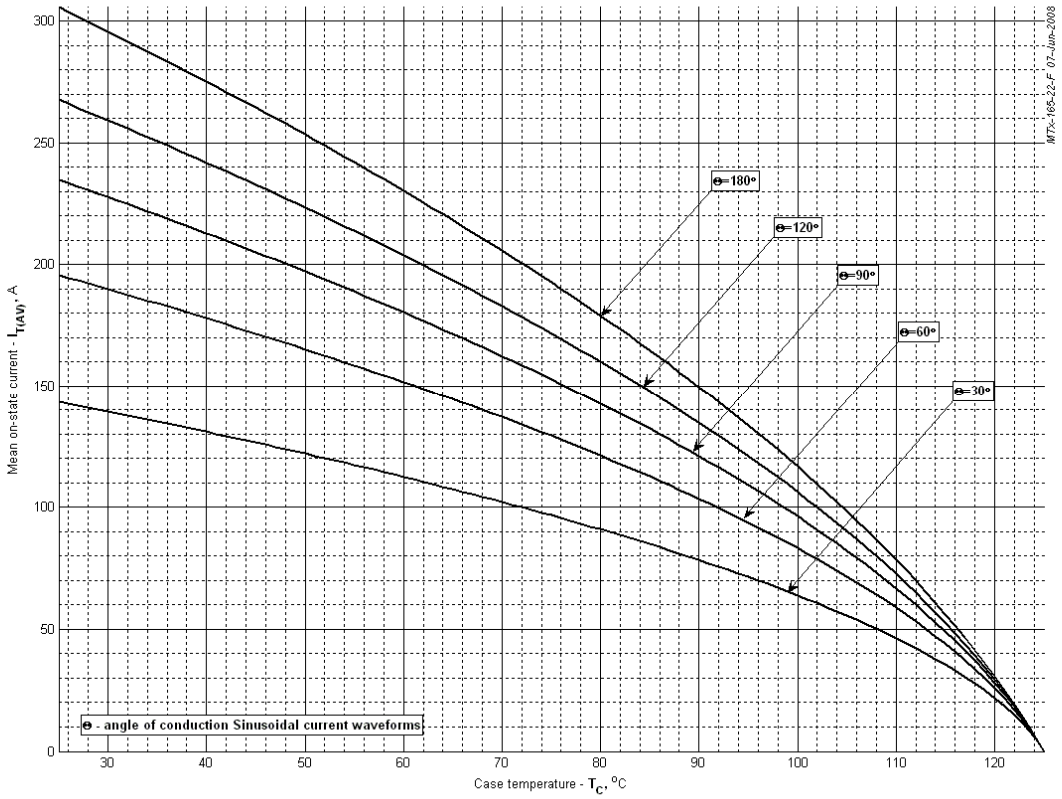


Fig 11 – Maximum case temperature (sinusoidal current waveforms)

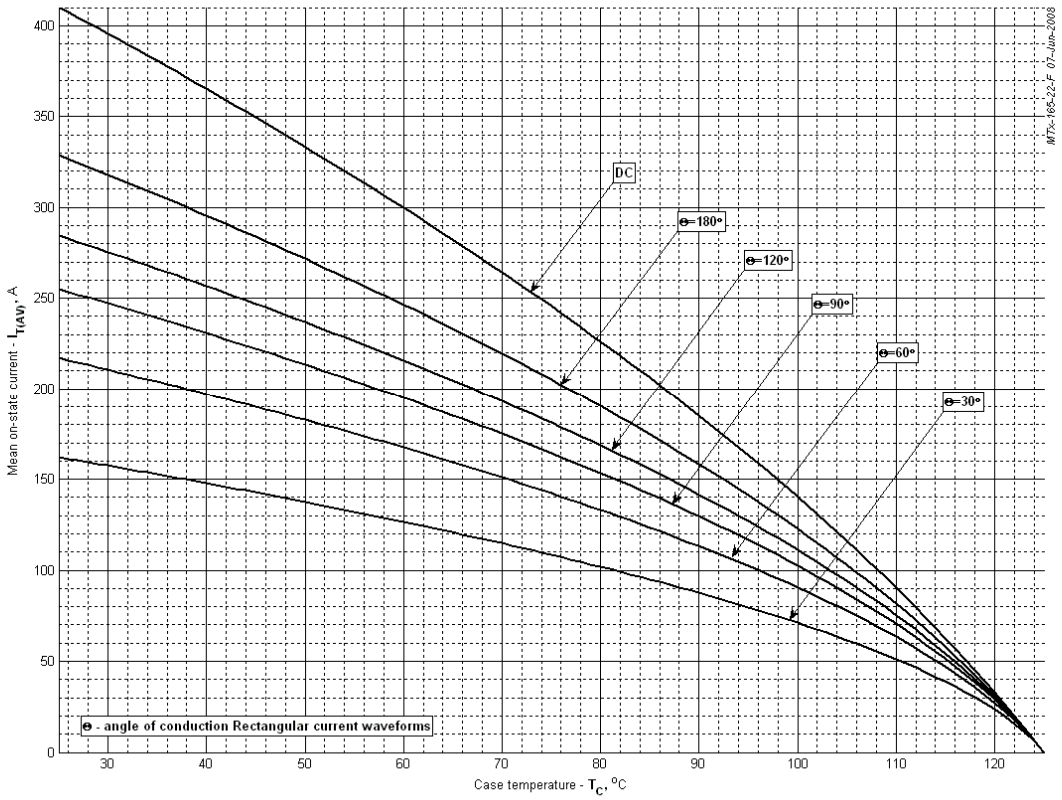


Fig 12 - Maximum case temperature (rectangular current waveforms)

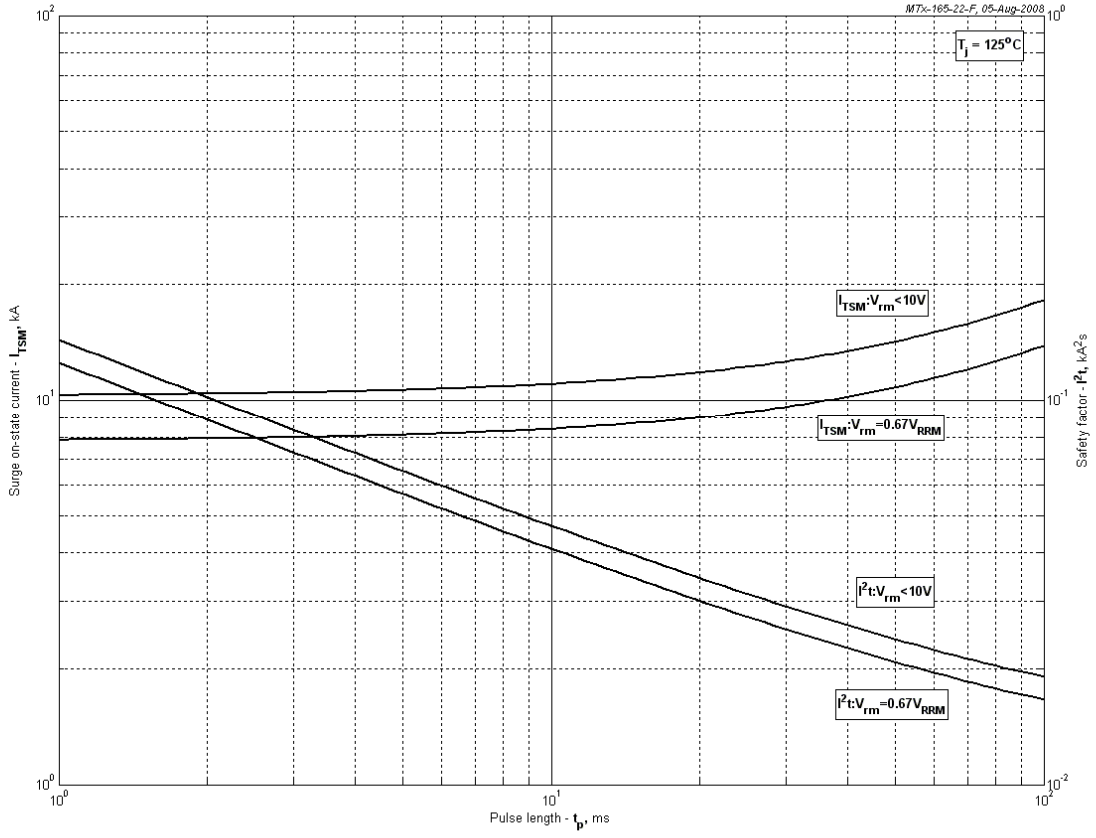


Fig 13 – Maximum surge and I^2t ratings

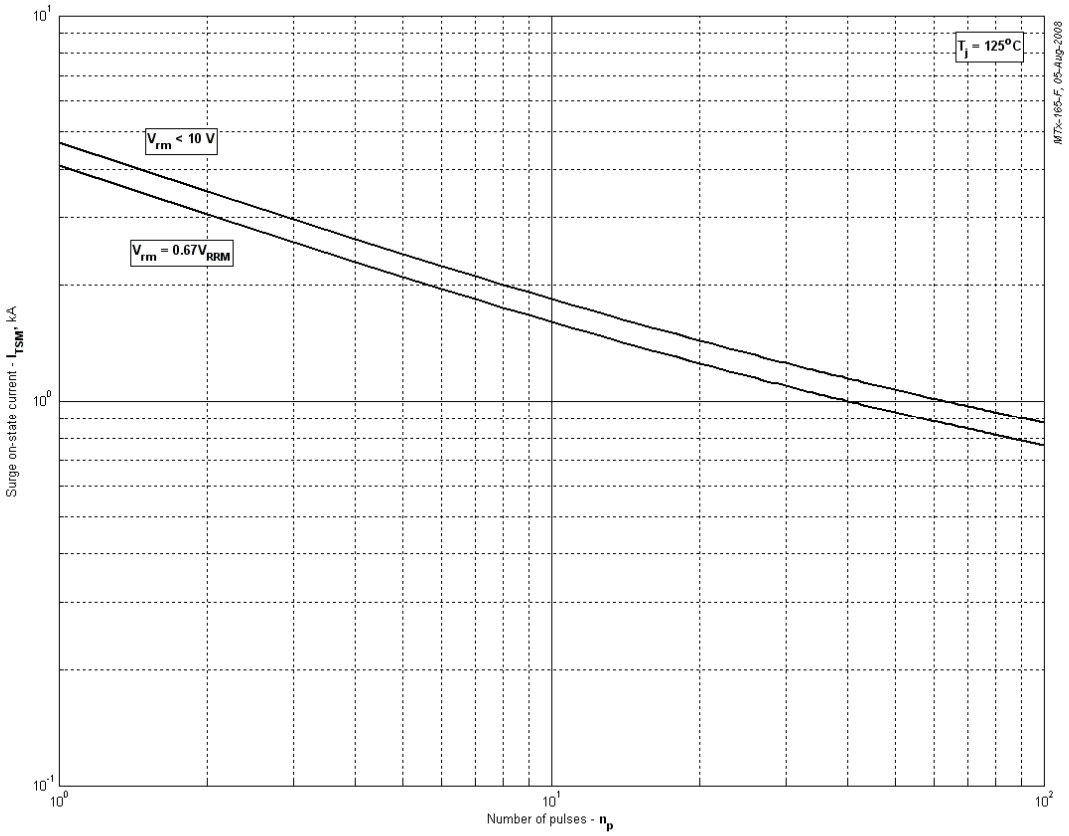


Fig 14 - Maximum surge ratings