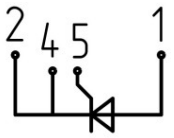
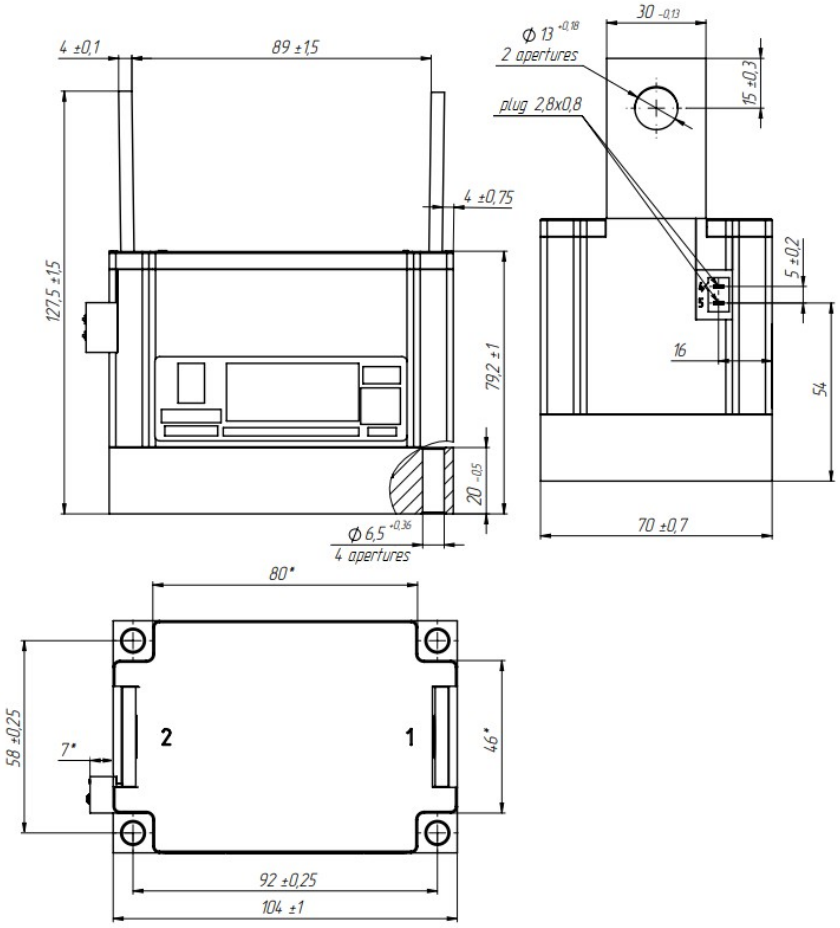
Single Thyristor Module For Phase Control MT1-560-36-E2M

Electrically isolated base plate
Industrial standard package
Simplified mechanical design, rapid assembly
Pressure contact

Maximum allowable mean on-state current		I_{TAV}	560 A	
Repetitive peak off-state voltage		V_{DRM}	3000...3600 V	
Repetitive peak reverse voltage		V_{RRM}		
Turn-off time		t_q	400 µs	
V_{DRM}, V_{RRM}, V	3000	3200	3400	3600
Voltage code	30	32	34	36
T_j, °C	–50...+125			

MT1





MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current	A	560 633	T_c=91 °C; T_c=85 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	879	T_c=91 °C; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	22.0 25.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=2 A; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
			23.0 26.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=2 A; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
I^2t	Safety factor	$A^2s\cdot10^3$	2400 3100	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=2 A; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
			2100 2800	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=2 A; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3000...3600	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3100...3700	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.6·V_{DRM} 0.6·V_{RRM}	T_j=$T_{j\,max}$; Gate open	
TRIGGERING					
I_{FGM}	Peak forward gate current	A	8	T_j=$T_{j\,max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	4	T_j=$T_{j\,max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	500	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; I_{TM}=1600 A; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs	
THERMAL					
T_{stg}	Storage temperature	°C	–50...+50		
T_j	Operating junction temperature	°C	–50...+125		
$T_{c\,op}$	Operating temperature	°C	–50...+125		
MECHANICAL					
a	Acceleration under vibration	m/s^2	50		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.90	T_j=25 °C; I_{TM}=2500 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.948	T_j=$T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	0.407		
I_L	Latching current, max	mA	1500	T_j=25 °C; V_D=12 V; Gate pulse: I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	250 4.00	T_j=$T_{j\,max}$ T_j= 25 °C	V_D=V_{DRM}; V_R=V_{RRM}
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/μs	200, 320, 500, 1000, 1600, 2000, 2500	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	T_j= $T_{j\,min}$ T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 250 150	T_j= $T_{j\,min}$ T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.50	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	70.00		
SWITCHING					
t_{gd}	Delay time, max	μs	1.40	T_j=25 °C; V_D=1500 V; I_{TM}=I_{TAV}; di/dt=200 A/μs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 μs; di_G/dt=2 A/μs	
t_{gt}	Turn-on time, max	μs	6.00		
t_q	Turn-off time[2], max	μs	400	dv_D/dt=50 V/μs; T_j=$T_{j\,max}$; I_{TM}= I_{TAV}; di_R/dt=-10 A/μs; V_R=100 V; V_D=0.67·V_{DRM}	
Q_{rr}	Recovered charge, max	μC	3910	T_j=$T_{j\,max}$; I_{TM}=500 A; di_R/dt=-5 A/μs; V_R=100 V	
t_{rr}	Reverse recovery time, max	μs	61		
I_{rr}	Reverse recovery current, max	A	128		
THERMAL					
R_{thjc}	Thermal resistance, junction to case			180° half-sine wave, 50 Hz	
	per module	°C/W	0.0400		
R_{thch}	Thermal resistance, case to heatsink				
	per module	°C/W	0.0100		
INSULATION					
V_{ISOL}	Insulation test voltage	kV	7.00	Sine wave, 50 Hz; RMS	t=60 sec
			8.40		t=1 sec
MECHANICAL					
M_1	Mounting torque (M6)[3]	Nm	6.00	Tolerance ± 15%	
M_2	Terminal connection torque (M12)[3]	Nm	18.00	Tolerance ± 15%	
m	Weight, max	g	2750		

PART NUMBERING GUIDE

MT	1	-	560	-	36	-	A2	H2	-	E2M	-	N
	1		2		3		4		5	6	7	8

1. MT - Thyristor module
2. Circuit Schematic:
3. Average On-state Current, A
4. Voltage Code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time (dv_D/dt=50 V/μs)
7. Package Type (M.E2M)
8. Ambient Conditions:
   N – Normal[4)]

NOTES

[1)] Critical rate of rise of off-state voltage

Symbol of Group	P2	K2	E2	A2	T1	P1	M1
$(dv_D/dt)_{crit}$, V/μs	200	320	500	1000	1600	2000	2500

[2)] Turn-off time (dv_D/dt=50 V/μs)

Symbol of Group	H2
t_q, μs	400

[3)] The screws must be lubricated

[4)] Additionally:
- ambient operating temperature –50...+60 °C;
- maximum altitude above sea level 1700 meters;
- frost and dew resistance.

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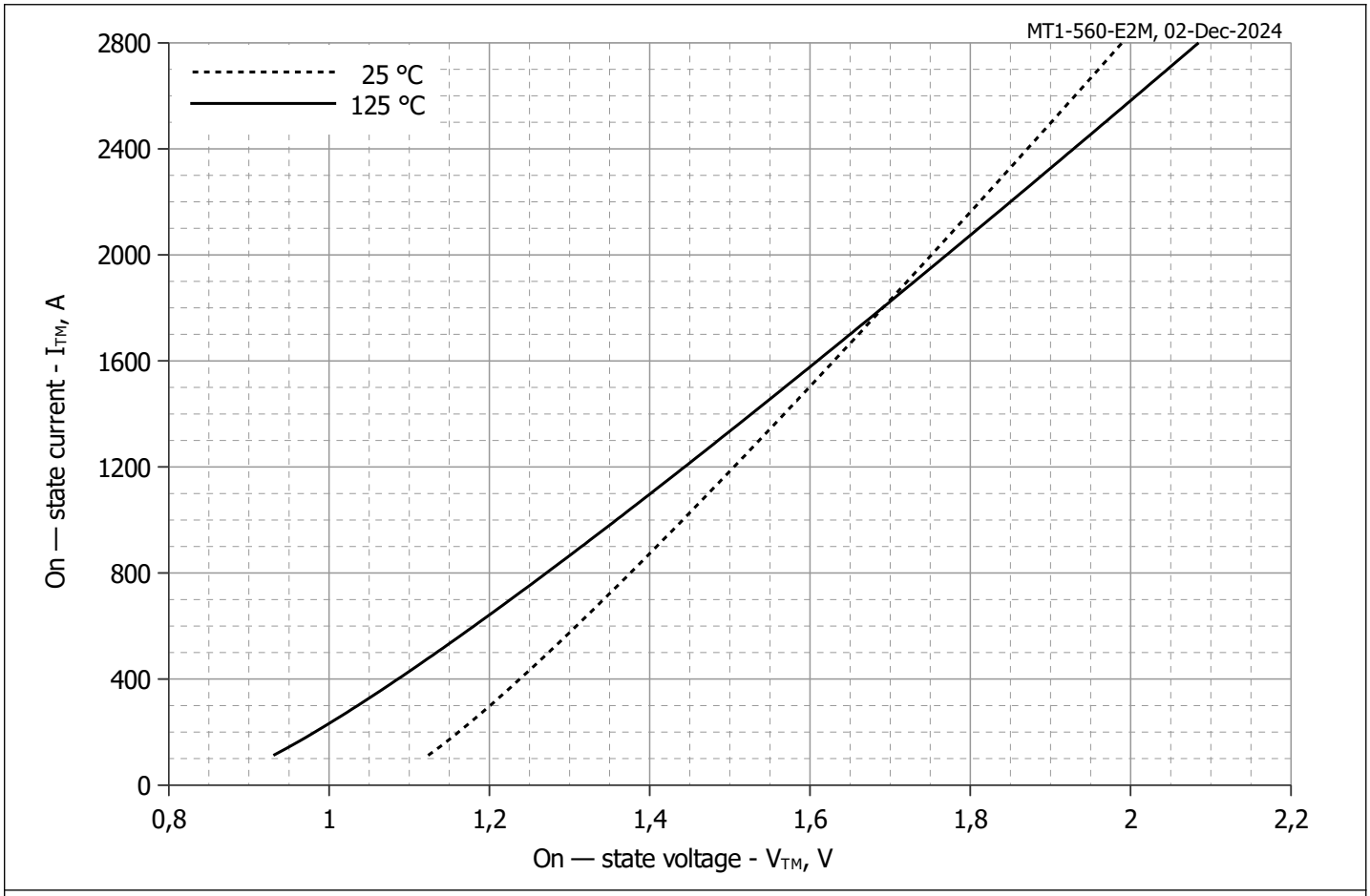

Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	$T_j = T_{j\,max}$
A	1.05284828	0.83406998
B	0.00024983	0.00032169
C	-0.00146269	-0.00304789
D	0.00469749	0.00707038

On-state characteristic model (see Fig. 1)

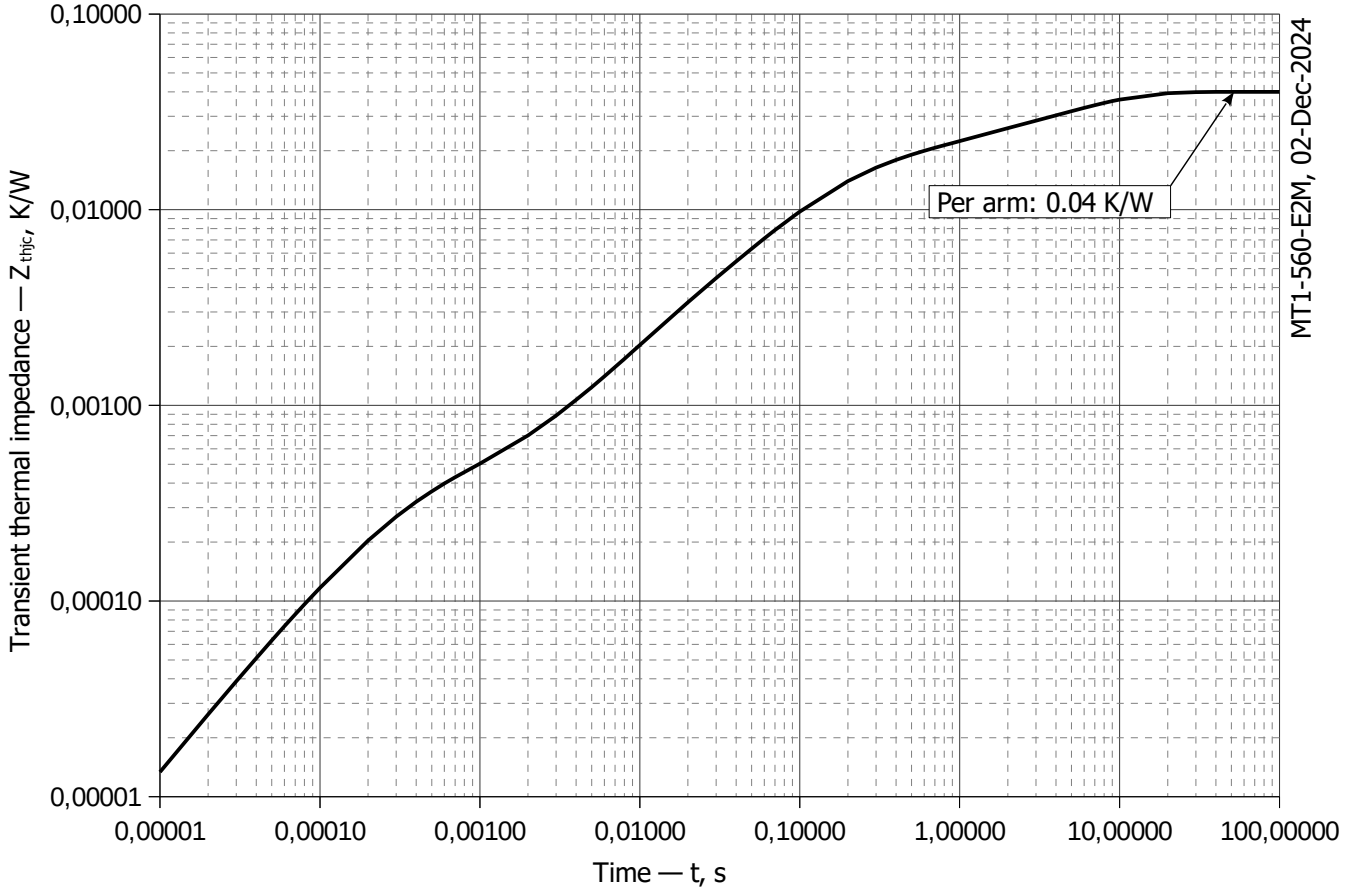

Fig 2 – Transient thermal impedance Z_{thjc} vs. time t

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t.

R_i = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

i	1	2	3	4	5	6
R_i, K/W	0.0189958	0.005931	0.009502	0.004252	0.001006	0.0003132
τ_i, s	5.887	0.7389	0.1616	0.08215	0.01267	0.0002712

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

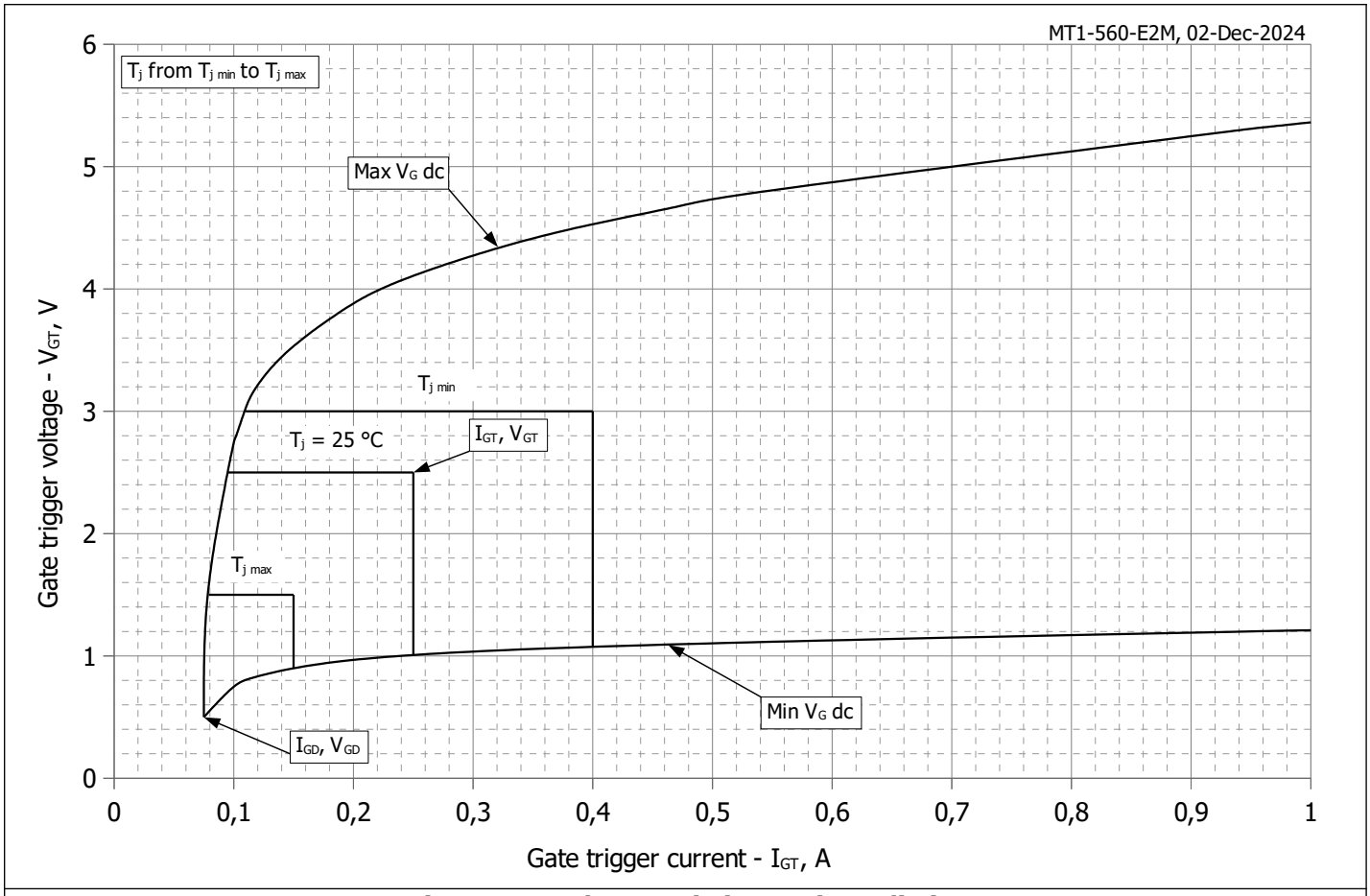

Fig 3 – Gate characteristics – Trigger limits

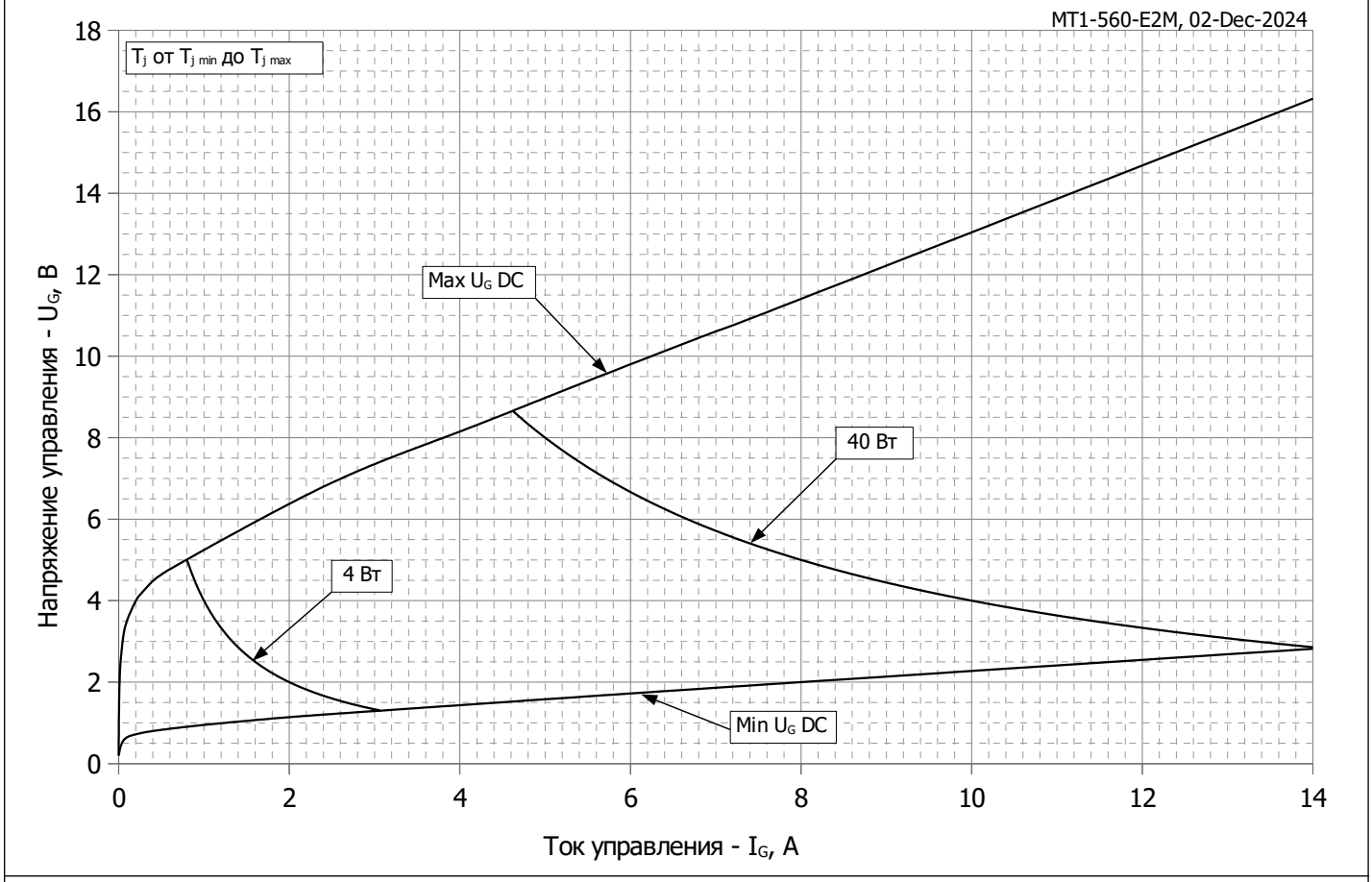

Fig 4 - Gate characteristics –Power curves

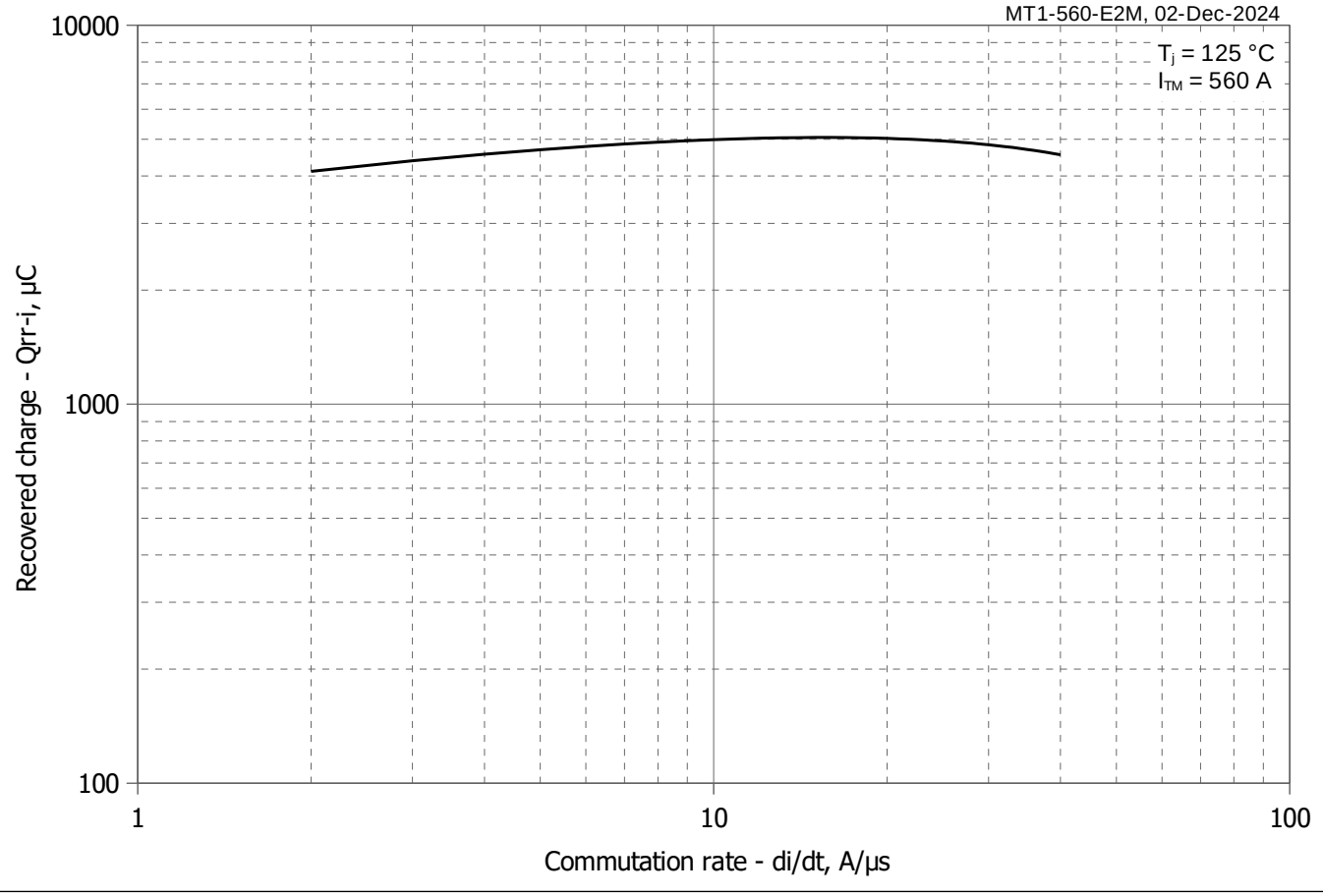

Fig 5 – Maximum recovered charge Q_{rr-i} (integral) vs. commutation rate di_R/dt

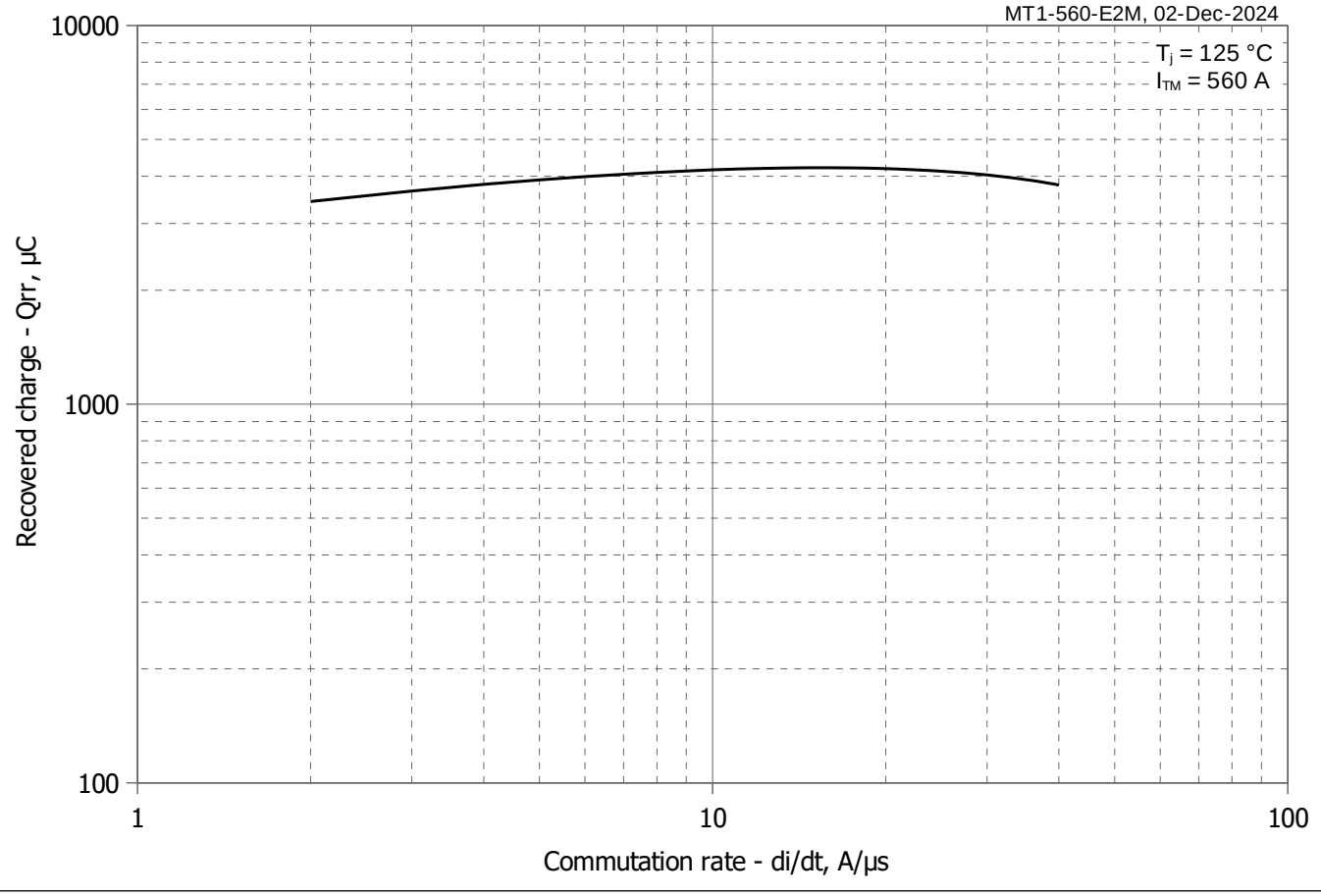

Fig 6 – Maximum recovered charge Q_{rr} vs. commutation rate di_R/dt (25% chord)

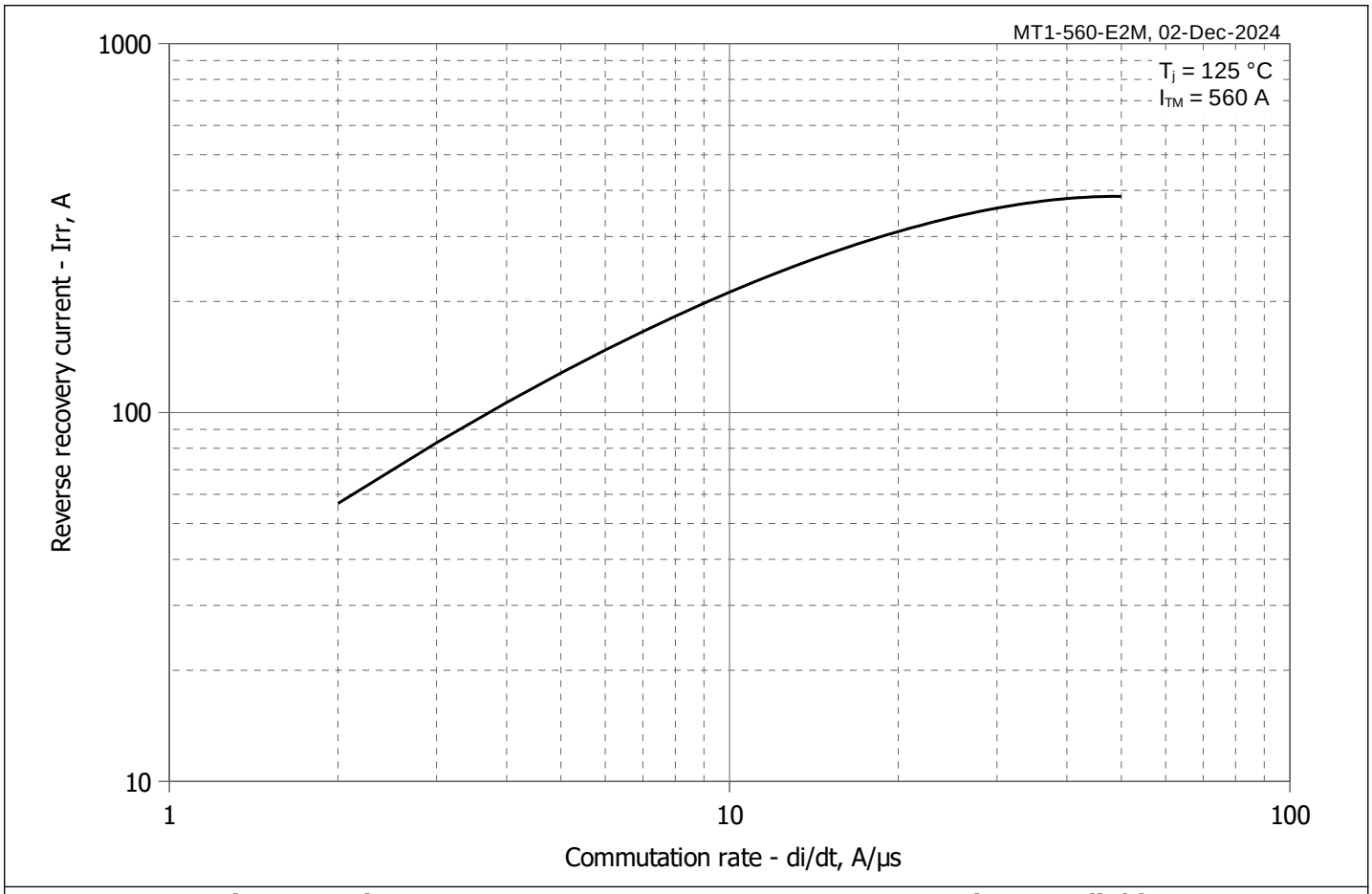

Fig 7 – Maximum reverse recovery current I_{rr} vs. commutation rate di_R/dt

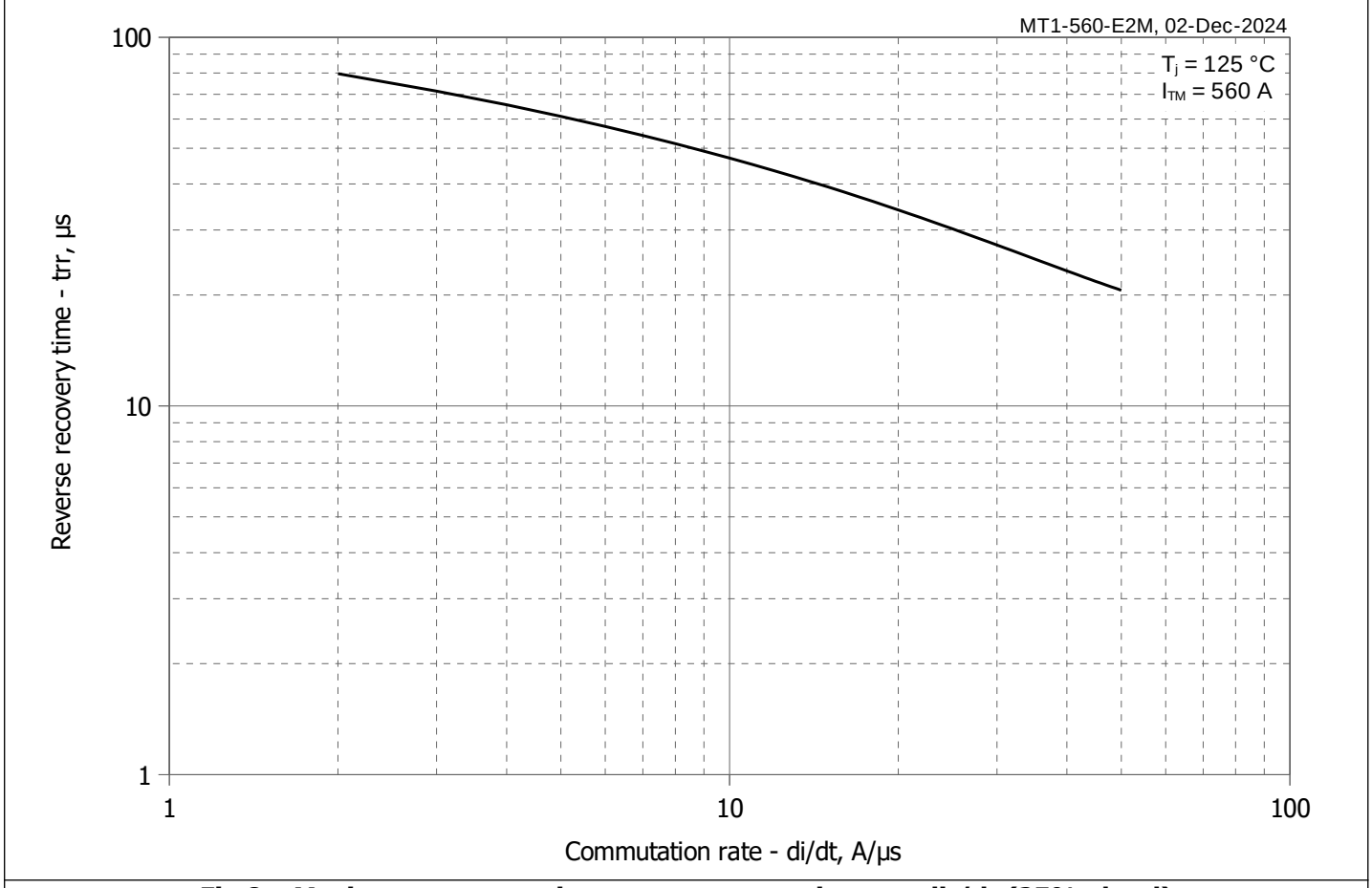

Fig 8 – Maximum recovery time t_{rr} vs. commutation rate di_R/dt (25% chord)

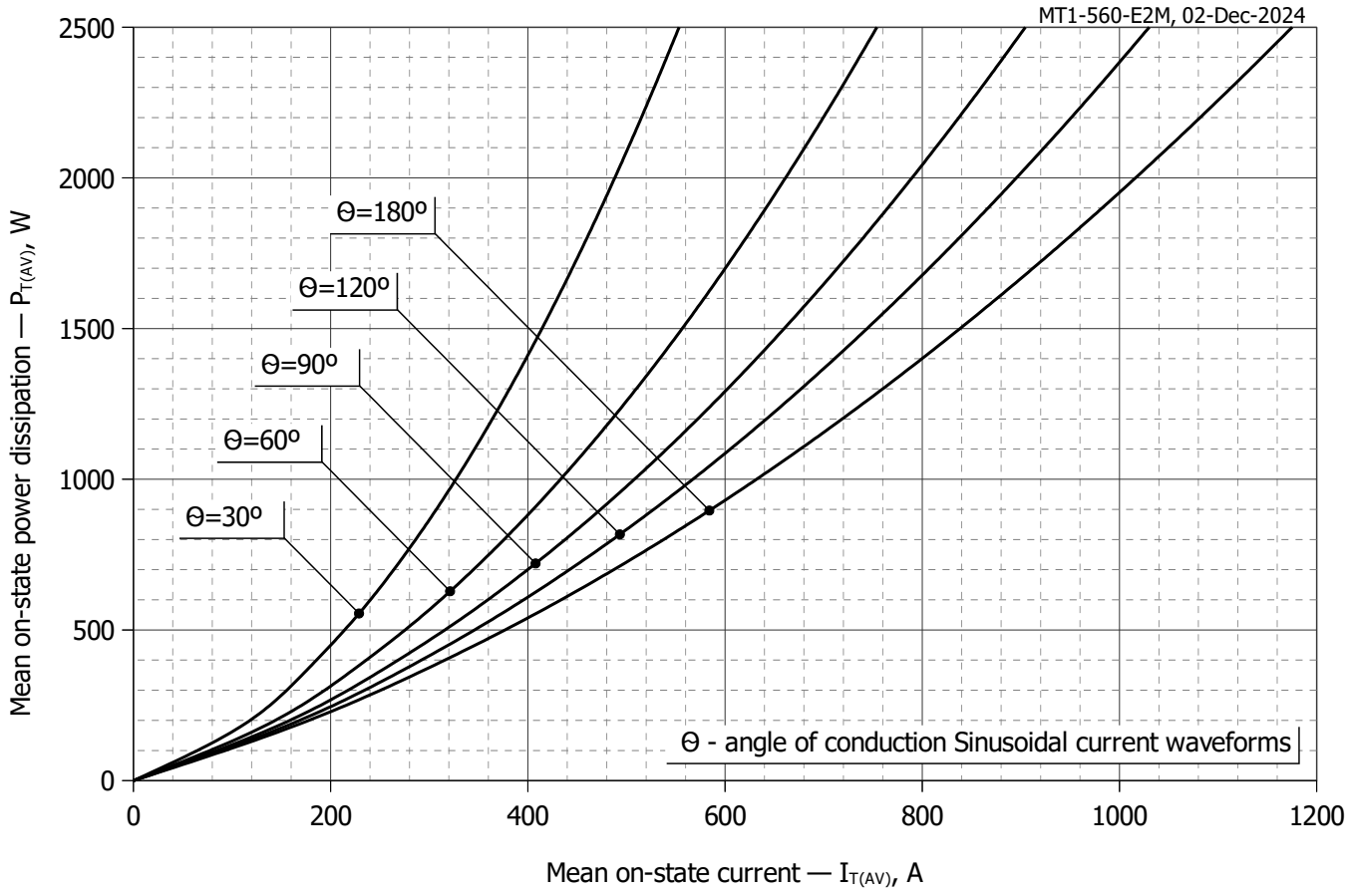

Fig. 9 - Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for sinusoidal current waveforms at different conduction angles (f=50Hz)

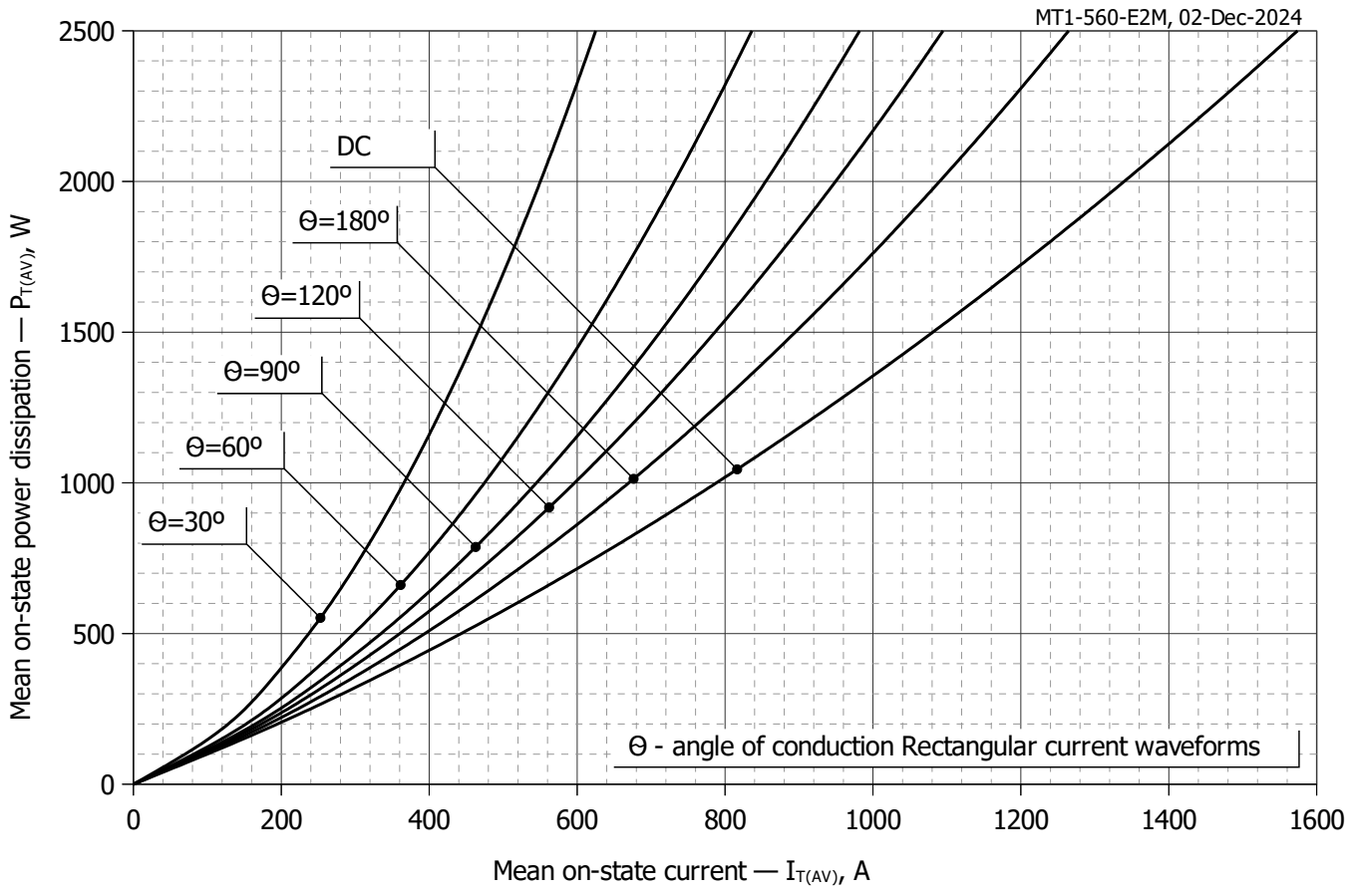

Fig. 10 – Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for rectangular current waveforms at different conduction angles and for DC (f=50Hz)

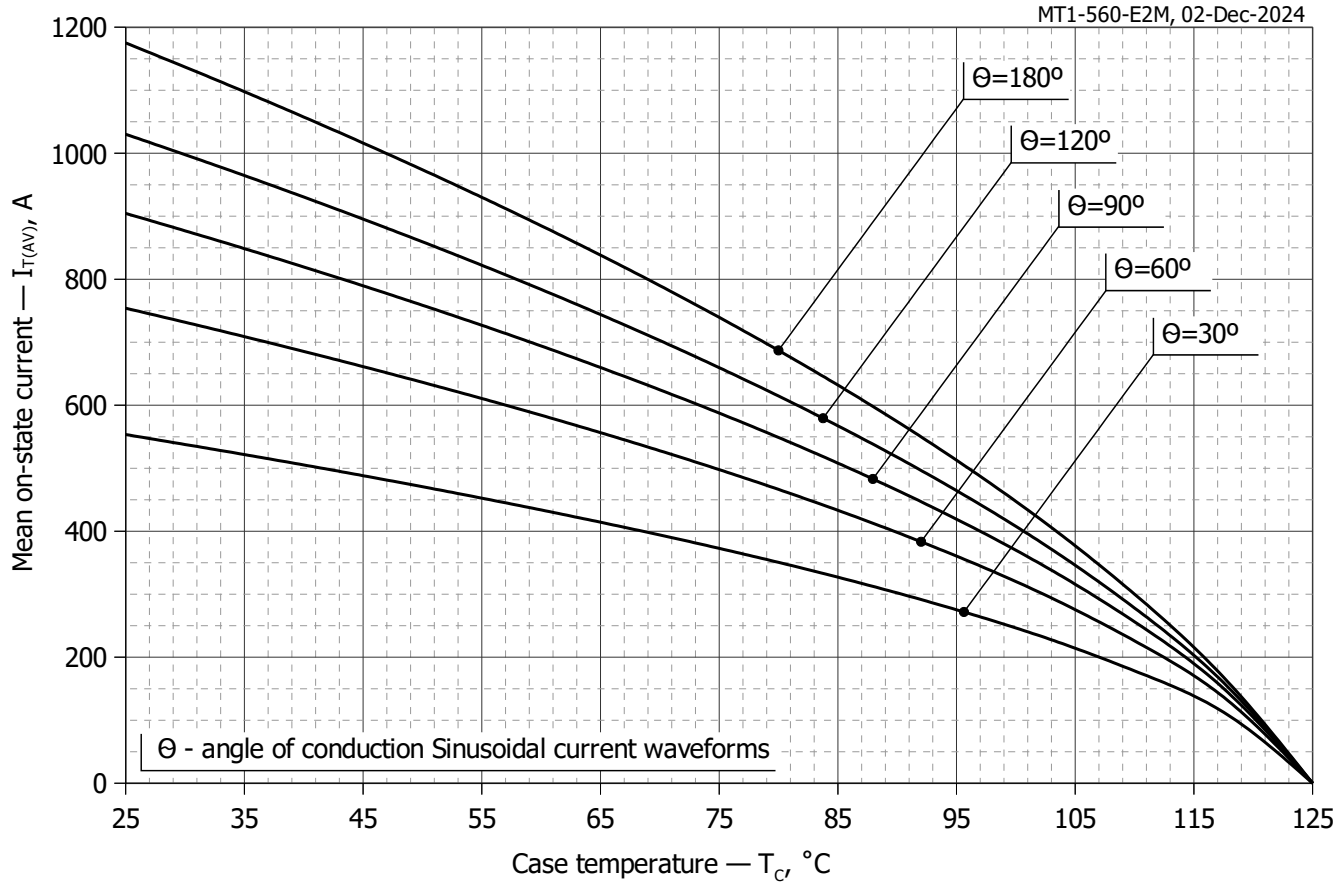

Fig. 11 – Mean on-state current I_{TAV} vs. case temperature T_C for sinusoidal current waveforms at different conduction angles (f=50Hz)

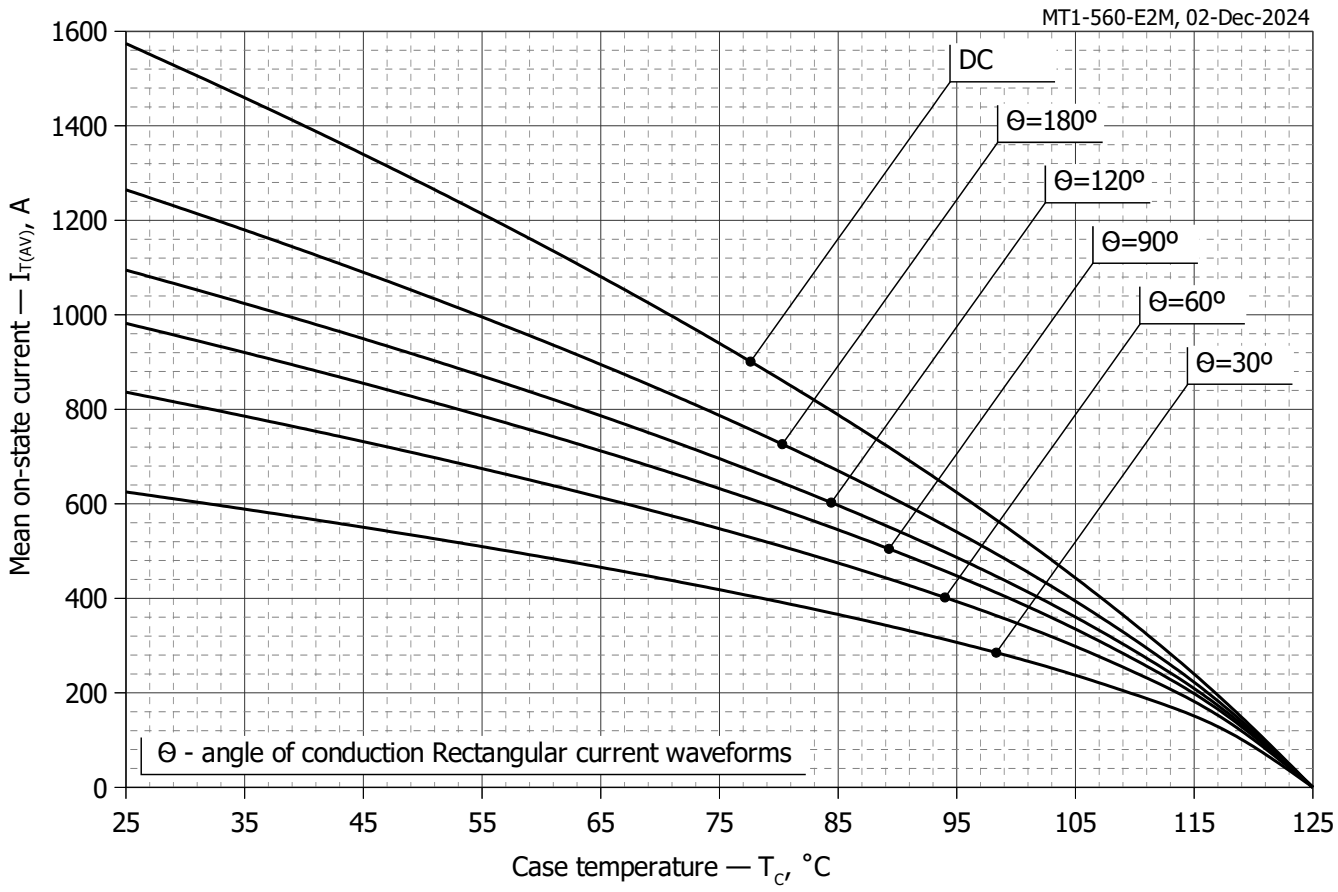

Fig. 12 - Mean on-state current I_{TAV} vs. case temperature T_C for rectangular current waveforms at different conduction angles and for DC (f=50Hz)

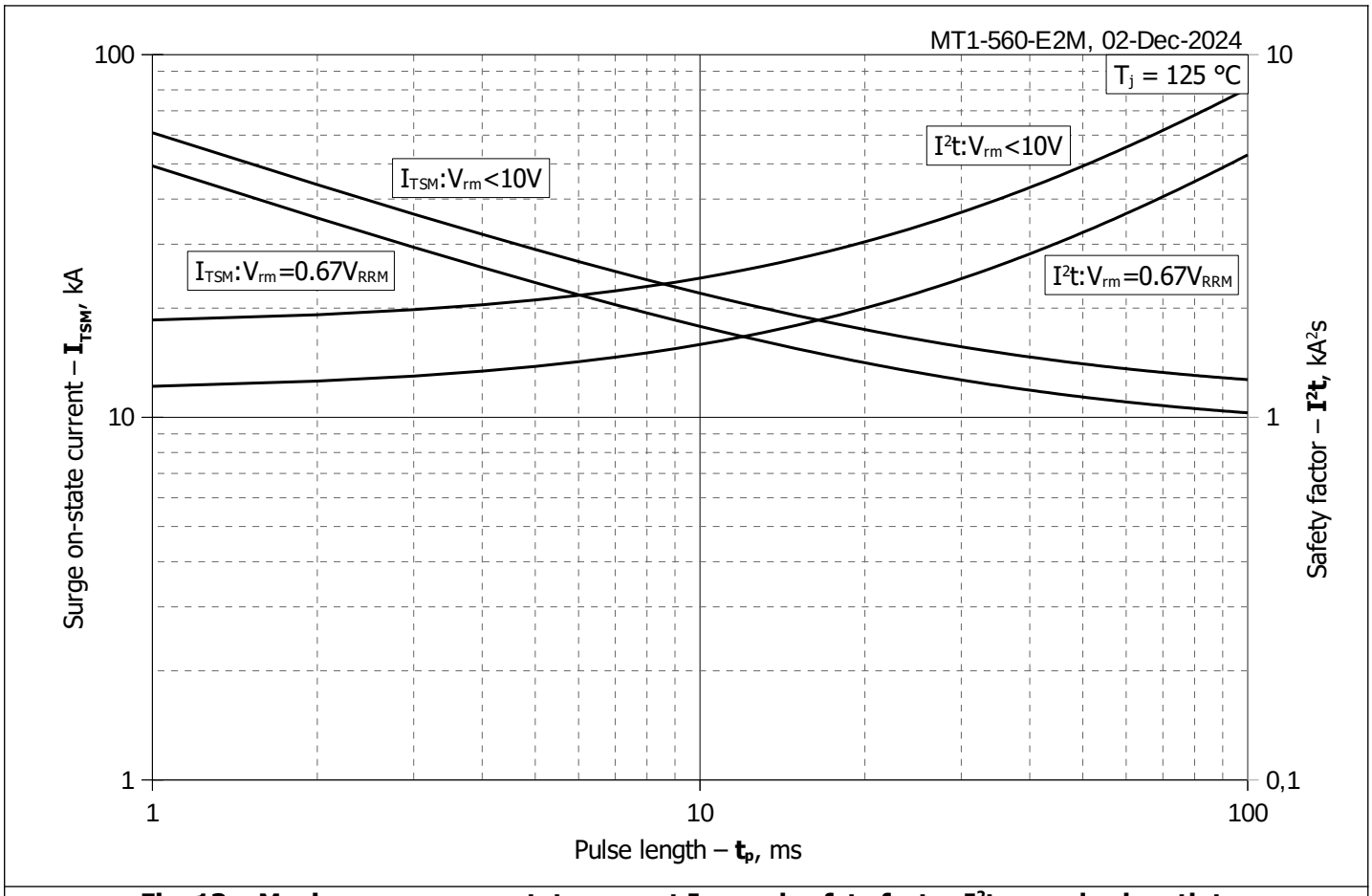

Fig. 13 – Maximum surge on-state current I_{TSM} and safety factor I^2t vs. pulse length t_p

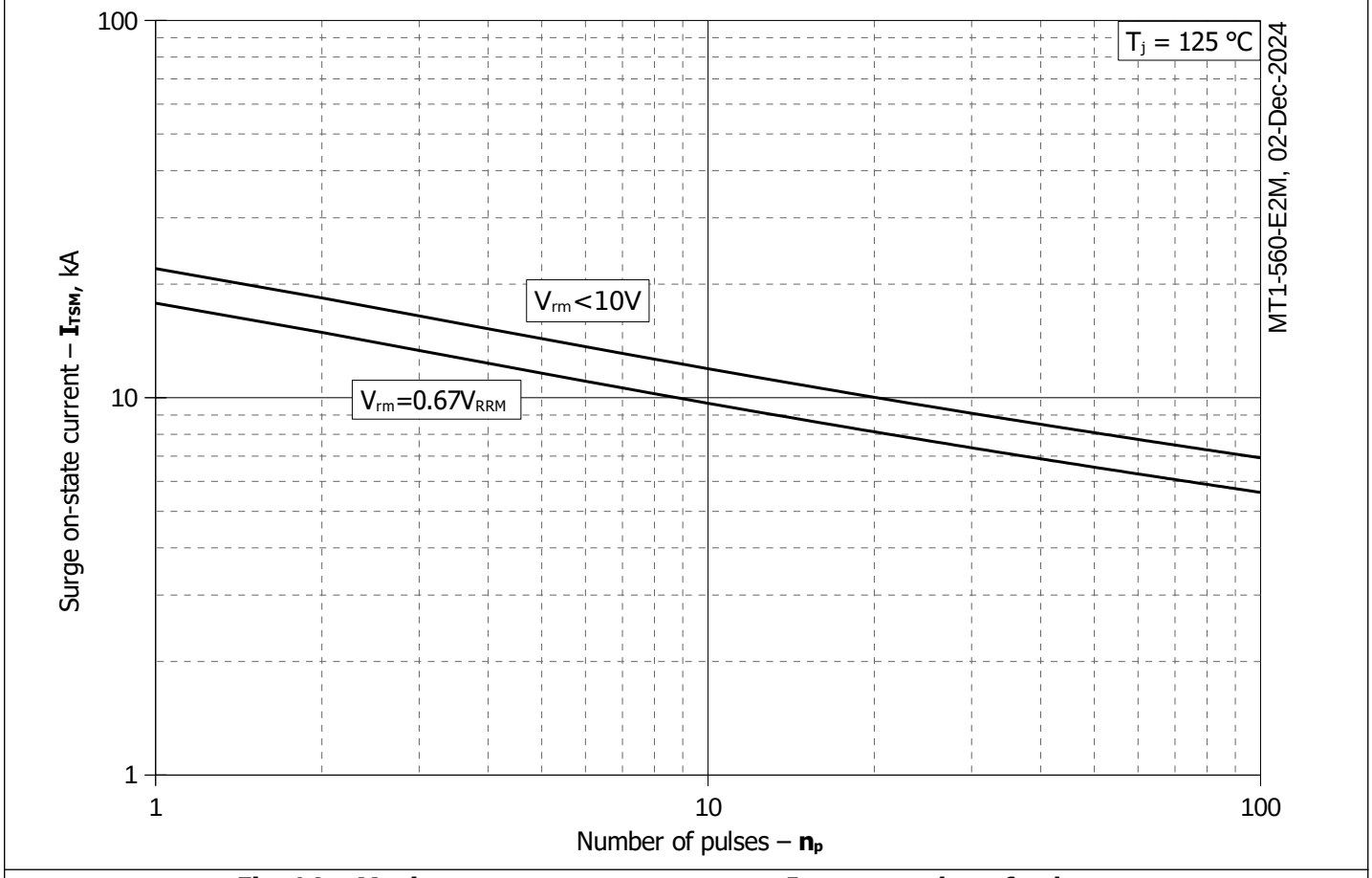

Fig. 14 - Maximum surge on-state current I_{TSM} vs. number of pulses n_p